8. Introduction to Micro-/Nanofabrication

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This chapter outlines and discusses important micro- and nanofabrication techniques. We start with the most basic methods borrowed from the integrated circuit (IC) industry, such as thin-film deposition, lithography and etching, and then move on to look at microelectromechanical systems (MEMS) and nanofabrication technologies. We cover a broad range of dimensions, from the micron to the nanometer scale. Although most of the current research is geared towards the nanodomain, a good understanding of top-down methods for fabricating micron-sized objects can aid our understanding of this research. Due to space constraints, we focus here on the most important technologies; in the microdomain these include surface, bulk, and high-aspect-ratio micromachining; in the nanodomain we concentrate on e-beam lithography, epitaxial growth, template manufacturing, and self-assembly. MEMS technology is maturing rapidly, with some new technologies displacing older ones that have proven to be unsuited to manufacture on a commercial scale. However, the jury is still out on methods used in the nanodomain, although it appears that bottom-up methods are the most feasible, and these will have a major impact in a variety of application areas such as biology, medicine, environmental monitoring, and nanoelectronics.

Recent innovations in the area of micro/nanofabrication have created a unique opportunity for manufacturing structures in the nm–mm range. The available six orders of magnitude dimensional span can be used to fabricate novel electronic, optical, magnetic, mechanical, and chemical/biological devices with applications ranging from sensors to computation and control. In this chapter, we will introduce major micro/nanofabrication techniques currently used to fabricate structures from the nm to several hundred μm range. We will mainly focus on the most important and widely used techniques and will not discuss specialized methods. After a brief introduction to basic microfabrication, we will discuss MEMS fabrication techniques used to build microstructures down to about 1 μm in dimensions. Following this, we will discuss several top-down and bottom-up nanofabrication methods not discussed in other chapters of this Handbook.

8.1 Basic Microfabrication Techniques

Most micro/nanofabrication techniques have their roots in the standard fabrication methods developed for the semiconductor industry [8.1–3]. Therefore, a clear understanding of these techniques is necessary for anyone starting to embark on a research and development path in the micro/nano area. In this section, we will discuss the major microfabrication methods used most frequently in the manufacturing of micro/nanostructures. Some of these techniques such as thin-film deposition and etching are common between the micro/nano and very large-scale integration (VLSI) microchip fabrication disciplines. However, several other techniques which are more specific to the micro/nanofabrication area will also be discussed in this section.

8.1.1 Lithography

Lithography is the technique used to transfer a computer-generated pattern onto a substrate (silicon, glass, GaAs, etc.). This pattern is subsequently used to etch an underlying thin film (oxide, nitride, etc.) for various purposes (doping, etching, etc.). Although photolithography, i. e., lithography using an ultraviolet (UV) light source, is by far the most widely used lithography technique in the microelectronic fabrication, electron-beam (e-beam) and x-ray lithography are two other alternatives which have attracted considerable attention in the MEMS and nanofabrication areas. We will discuss photolithography in this section and postpone discussion of e-beam and x-ray techniques to subsequent sections dealing with MEMS and nanofabrication.

The starting point subsequent to the creation of the computer layout for a specific fabrication sequence is the generation of a photomask. This involves a sequence of photographic processes (using optical or e-beam pattern generators), which results in a glass plate having the desired pattern in the form of a thin (≈ 100 nm) chromium layer. Following the generation of the photomask, the lithography process can proceed as shown in Fig. 8.1. This sequence demonstrates the pattern transfer onto a substrate coated with silicon dioxide; however, the same technique is applicable to other materials. After depositing the desired material on the substrate, the photolithography process starts with spin-coating the substrate with a photoresist. This is a polymeric photosensitive material which can be spun onto the wafer in liquid from (usually an adhesion promoter such as hexamethyldisilazane HMDS is used prior to the application of the resist). The spinning speed and photoresist viscosity will determine the final resist thickness, which is typically in the range 0.5–2.5 μm. Two different kinds of photoresist are available: positive and negative. With positive resist, UV-exposed areas will be dissolved in the subsequent development stage, whereas with negative photoresist, the exposed areas will remain intact after UV development. Due to its better performance with regard to process control in small geometries, positive resist is the most extensively used in the VLSI processes. After spinning the photoresist onto the wafer, the substrate is soft-baked (5–30 min at 60–100 °C) in order to remove the solvents from the resist and improve adhesion. Subsequently, the mask is aligned to the wafer and the photoresist is exposed to a UV source.

Depending on the separation between the mask and the wafer three different exposure systems are available:

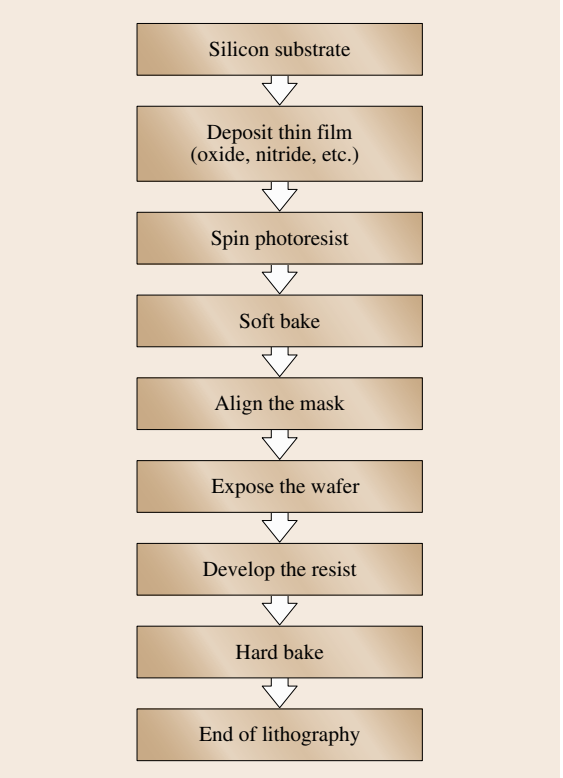

Fig. 8.1 Lithography process flow

1. Contact
2. Proximity
3. Projection

Although contact printing gives better resolution compared with the proximity technique, the constant contact of the mask with the photoresist reduces the process yield and can damage the mask. Projection printing uses a dual-lens optical system to project the mask image onto the wafer. Since only one die at a time can be exposed, this requires a step-and-repeat system to cover the whole wafer area. Projection printing is by far the most widely used system in microfabrication and can yield superior resolutions compared with the contact and proximity methods. The exposure source for photolithography depends on the resolution. Above 0.25 μm minimum line width, a high-pressure mercury lamp is adequate (436 nm g-line and 365 nm i-line). However, between 0.25 and 0.13 μm, deep-UV sources such as excimer lasers (248 nm KrF and 193 nm ArF) are required. Although there has been extensive competition for the below-0.13 μm regime (including e-beam and x-ray), extreme UV (EUV) with wavelength of 10–14 nm seems to be the preferred technique, although major technical challenges still remain [8.4]. Immersion lithography (i. e., using a liquid in the space between the lens and substrate in order to increase the numerical aperture), a recent innovation, has allowed the minimum feature size to be reduced to 32 nm without the requirement for EUV sources [8.5].

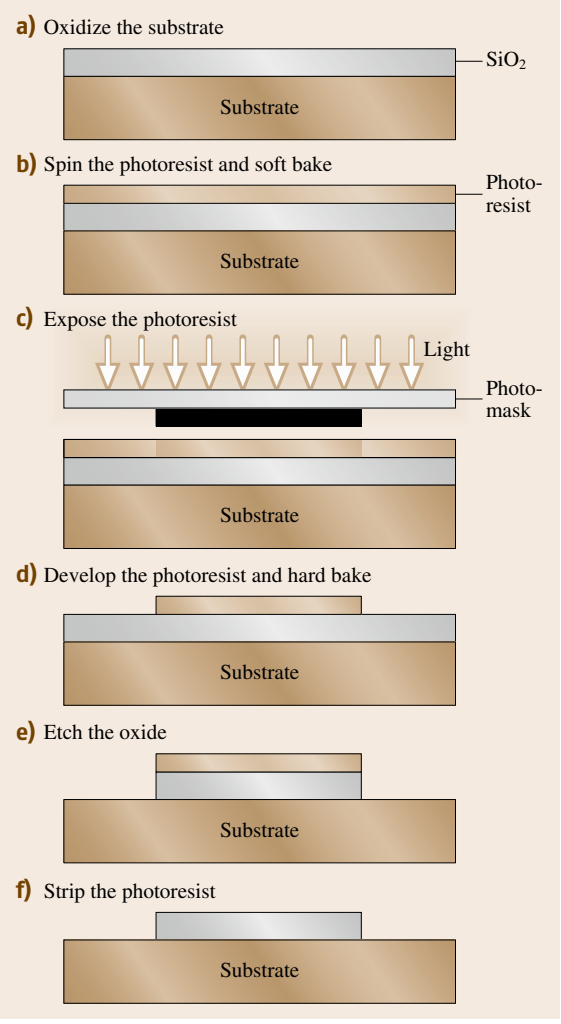

Fig. 8.2a–f Schematic drawing of the photolithographic steps with a positive PR

After exposure, the photoresist is developed in a process similar to the development of photographic films. The resist is subsequently hard-baked (20–30 min at 120–180 °C) in order to further improve adhesion. The hard-bake step concludes the photolithography sequence by creating the desired pattern on the wafer. Next, the underlying thin film is etched and the photoresist is stripped using acetone or other organic removal solvents. Figure 8.2 shows a schematic of the photolithography steps with a positive photoresist.

8.1.2 Thin-Film Deposition and Doping

Thin-film deposition and doping are extensively used in micro/nanofabrication technologies. Most fabricated micro/nanostructures contain materials other than that of the substrate, which are obtained by various deposition techniques or by modification of the substrate. Following is a list of a few typical applications for the deposited and/or doped materials used in micro/nanofabrication, which gives an idea of the required properties:

- Mechanical structure
- Electrical isolation
- Electrical connection
- Sensing or actuating
- Mask for etching and doping
- Support or mold during deposition of other materials (sacrificial materials)
- Passivation

Most of the deposited thin films have properties different from those of their corresponding *bulk* forms (for example, metals shows higher resistivities in thin-film

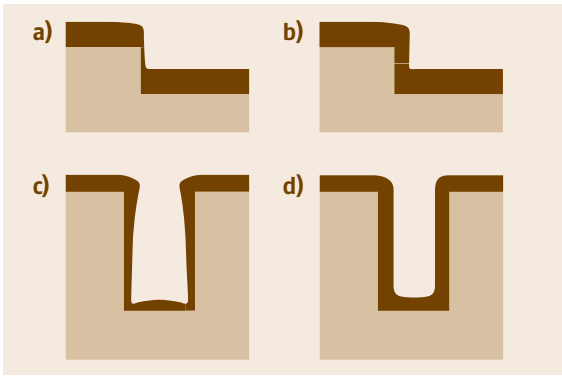

Fig. 8.3a–d Step coverage and conformality: **(a)** poor step coverage, **(b)** good step coverage, **(c)** nonconformal layer, and **(d)** conformal layer

form). In addition, the techniques utilized to deposit these materials have a great impact on their final properties. For instance, internal stress (compressive or tensile) in a film is strongly process dependent. Excessive stress may crack or detach the film from the substrate and therefore must be minimized, although it may also be useful for certain applications. Adhesion is another important issue that needs to be taken into account when depositing thin films. In some cases such as the deposition of noble metals (e.g., gold) an intermediate layer (chromium or titanium) may be needed to improve adhesion. Finally, step coverage and conformality are two properties that can also influence the choice of one or another deposition technique. Figure 8.3 illustrates these concepts.

Oxidation

Oxidation of silicon is a process used to obtain a thin film of SiO_2 with excellent quality (very low density of defects) and thickness homogeneity. Although it is not properly a deposition, the result is the same; i. e., a thin layer of a new material covering the surface is produced. The oxidation process is typically carried out at temperatures in the range of 900–1200 °C in the presence of O_2 (dry oxidation) or H_2O (wet oxidation). The reactions for oxide formation are

$$Si_{(solid)} + O_{2\,(gas)} \Rightarrow SiO_{2\,(solid)}$$

and

$$Si_{(solid)} + 2H_2O_{(steam)} \Rightarrow SiO_{2\,(solid)} + 2H_{2\,(gas)} \,.$$

Although the rate of oxide growth is higher for wet oxidation, this is achieved at the expense of lower oxide

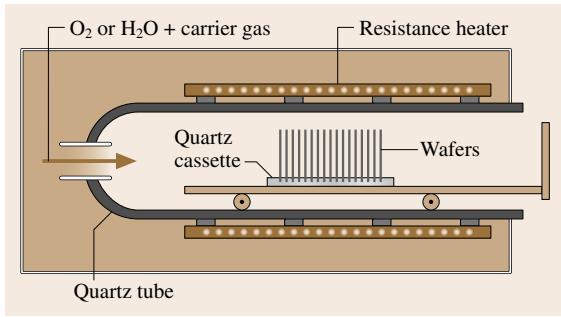

Fig. 8.4 Schematic representation of a typical oxidation furnace

quality (density). Since silicon atoms from the substrate participate in the reaction, the substrate is consumed as the oxide grows (≈ 44% of the total thickness lies above the line of the original silicon surface). The oxidation of silicon also occurs at room temperature, however a layer of about 20 Å (native oxide) is enough to passivate the surface and prevent further oxidation. To grow thicker oxides, wafers are introduced into an electric resistance furnace such as that represented in Fig. 8.4. Tens of wafers can be processed in a single batch in such equipment. By strictly controlling the timing, temperature, and gas flow entering the quartz tube the desired thickness can be achieved with high accuracy. Thicknesses ranging from a few tens of Angstroms to 2 µm can be obtained in reasonable times. Despite the good quality of the SiO_2 obtained by silicon oxidation (also called *thermal oxide*), the use of this process is often limited to the early stages of the fabrication, since some of the materials added during the formation of structures may not withstand the high temperatures. The contamination of the furnace, when the substrates have been previously in contact with certain etchants such as KOH or when materials such as metals have been deposited, also poses limitations in most cases.

Doping

The introduction of certain impurities in a semiconductor can change its electrical, chemical, and even mechanical properties. Typical impurities or *dopants* used in silicon include boron (to form p-type regions) and phosphorous or arsenic (to form n-type regions). Doping is the main process used in the microelectronic industry to fabricate major components such as diodes and transistors. In micro/nanofabrication technologies doping has additional applications such as the formation of piezoresistors for mechanical transducers or the creation of etch stop-layers. Two different techniques

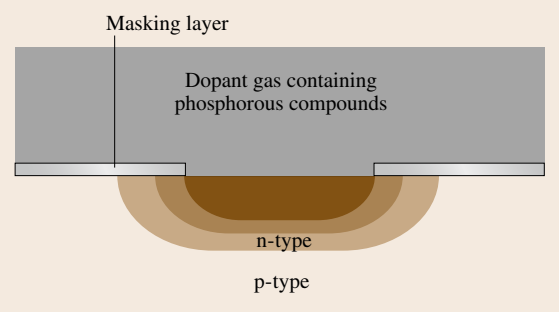

Fig. 8.5 Formation of an n-type region on a p-type silicon substrate by diffusion of phosphorous

are used to introduce impurities into a semiconductor substrate: diffusion and ion implantation.

Diffusion is the process which became dominant in the initial years following the invention of the integrated circuit to form n- and p-type regions in the silicon. The diffusion of impurities into silicon occurs only at high temperature (above 800 °C). Furnaces used to carry out this process are similar to those used for oxidation. Dopants are introduced in the furnace gaseous atmosphere from liquid or solid sources. Figure 8.5 illustrates the process of creating an n-type region by diffusion of phosphor from the surface into a p-type substrate. A masking material is previously deposited and patterned on the surface to define the areas to be doped. However, because diffusion is an isotropic process, the doped area will also extend underneath the mask. In microfabrication, diffusion is mainly used for the formation of very highly boron-doped regions (p^{++}), which are usually used as an etch stop in bulk micromachining.

Ion implantation allows more precise control of the dose (the total amount of impurities introduced per area unit) and the impurity profile (the concentration versus depth). In ion implantation the impurities are ionized and accelerated towards the semiconductor surface. The penetration of impurities into the material follows a Gaussian distribution. After implantation, an annealing process is needed to activate the impurities and repair the damage in the crystal structure produced by ion collisions. A *drive-in* process to redistribute the impurities, done in a standard furnace such as those used for oxidation or diffusion, may be required as well.

Chemical Vapor Deposition and Epitaxy

As its name suggests, chemical vapor deposition (CVD) includes all deposition techniques using the reaction of chemicals in gas phase to form the deposited thin film. The energy needed for the chemical reaction to occur is usually supplied by maintaining the substrate at elevated temperature. Alternative energy sources such as plasma or optical excitation are also used, with the advantage of requiring a lower temperature at the substrate. The most common CVD processes in microfabrication are low-pressure CVD (LPCVD) and plasma-enhanced (PECVD).

The LPCVD process is typically carried out in electrically heated tubes, similar to oxidation tubes, equipped with pumping capabilities to achieve the low pressures required (0.1–1.0 Torr). Large numbers of wafers can be processed simultaneously and the material is deposited on both sides of the wafers. The process temperature depends on the material to be deposited, but generally is in the range 550–900 °C. As in oxidation, high temperatures and contamination issues can restrict the type of processes used previous to the LPCVD. Typical materials deposited by LPCVD include silicon oxide (e.g., $SiCl_2H_2 + 2N_2O \Rightarrow SiO_2 + 2N_2 + 2HCL$ at 900 °C), silicon nitride (e.g., $3SiH_4 + 4NH_3 \Rightarrow Si_3N_4 + 12H_2$ at 700–900 °C), and polysilicon (e.g., $SiH_4 \Rightarrow Si + 2H_2$ at 600 °C). Due to its faster etch rate in HF, in situ phosphorous-doped LPCVD oxide (phosphosilicate glass, PSG) is extensively used in surface micromachining as the sacrificial layer. Conformality in this process is excellent, even for very high-aspect-ratio structures. Mechanical properties of LPCVD materials are good compared with others such as PECVD, and are often used as structural materials in microfabricated devices. Stress in the deposited layers depends on the material, deposition conditions, and subsequent thermal history (e.g., postdeposition annealing). Typical values are: 100–300 MPa (compressive) for oxide, ≈ 1 GPa (tensile) for stoichiometric nitride, and ≈ 200–300 MPa (tensile) for polysilicon. The stress in nitride layers can be reduced to nearly zero by using a silicon-rich composition. Since the stress values can vary over a wide range, one has to measure and characterize the internal stress of deposited thin films for any specific equipment and deposition conditions.

The PECVD process is performed in plasma systems such as that represented in Fig. 8.6. The use of radiofrequency (RF) energy to create highly reactive species in the plasma allows for the use of lower temperature at the substrate (150–350 °C). Parallel-plate plasma reactors normally used in microfabrication can only process a limited number of wafers per batch. The wafers are positioned horizontally on top of the lower electrode so only one side gets deposited. Typical materials deposited with PECVD include silicon oxide,

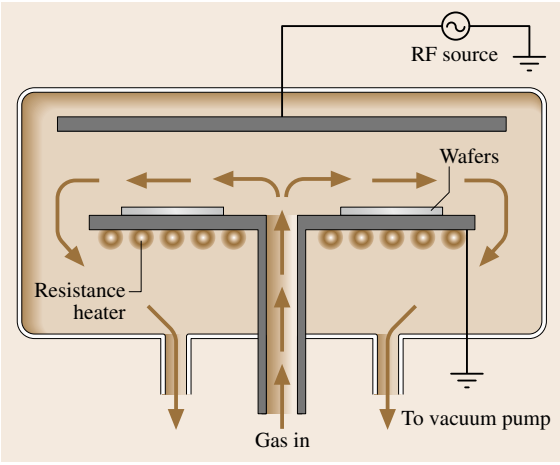

Fig. 8.6 Schematic representation of a typical PECVD system

nitride, and amorphous silicon. Conformality is good for low-aspect-ratio structures, but becomes very poor for deep trenches (20% of the surface thickness inside through-wafer holes with an aspect ratio of 10). Stress depends on deposition parameters and can be either compressive or tensile. PECVD nitrides are typically nonstoichiometric (Si_xN_y) and are much less resistant to etchants in masking applications.

Another interesting type of CVD is epitaxial growth. In this process, a single-crystalline material is grown as an extension of the crystal structure of the substrate. It is possible to grow dissimilar materials if the crystal structures are somehow similar (lattice matched). Silicon-on-sapphire (SoS) substrates and some heterostructures are fabricated in this way. However, most common in microfabrication is the growth of silicon on another silicon substrate. Of particular interest for the formation of microstructures is selective epitaxial growth. In this process the silicon crystal is allowed to grow only in windows patterned on a masking material. Many CVD techniques have been used to produce epitaxial growth. The most common for silicon is thermal chemical vapor deposition or vapor-phase epitaxy (VPE). Metalorganic chemical vapor deposition (MOCVD) and molecular-beam epitaxy (MBE) are the most common for growing high-quality III–V compound layers with nearly atomic abrupt interfaces. The former uses vapors of organic compounds with group III atoms such as trimethylgallium ($Ga(CH_3)_3$) and group V hydrides such as AsH_3 in a CVD chamber with fast gas switching capabilities. The latter typically uses molecular beams from thermally evaporated elemental sources aiming at the substrate in an ultrahigh-vacuum chamber. In this case, rapid on/off control of the beams is achieved by using shutters in front of the sources. Finally, it should be mentioned that many metals (molybdenum, tantalum, titanium, and tungsten) can also be deposited using LPCVD. These are attractive for their low resistivities and their ability to form silicides with silicon. Due to its application in new interconnect technologies, copper CVD is an active area of research.

Physical Vapor Deposition (Evaporation and Sputtering)

In physical deposition systems the material to be deposited is transported from a source to the wafers, both being in the same chamber. Two physical principles are used to do this: evaporation and sputtering.

In evaporation, the source is placed in a small container with tapered walls, called the crucible, and is heated up to a temperature where evaporation occurs. Various techniques are utilized to reach the high temperatures needed, including the induction of high currents with coils wound around the crucible and the bombardment of the material surface with an electron beam (e-beam evaporators). This process is mainly used to deposit metals, although dielectrics can also be evaporated. In a typical system the crucible is located at the bottom of a vacuum chamber whereas the wafers are placed lining the dome-shaped ceiling of the chamber (Fig. 8.7). The main characteristic of this process is very poor step coverage, including shadow effects as illustrated in Fig. 8.8. As will be explained in subsequent

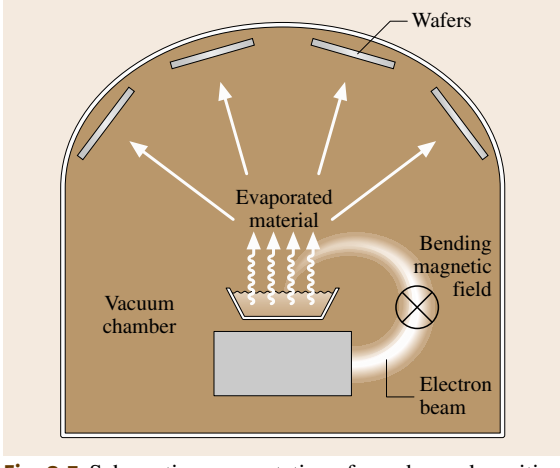

Fig. 8.7 Schematic representation of an e-beam deposition system

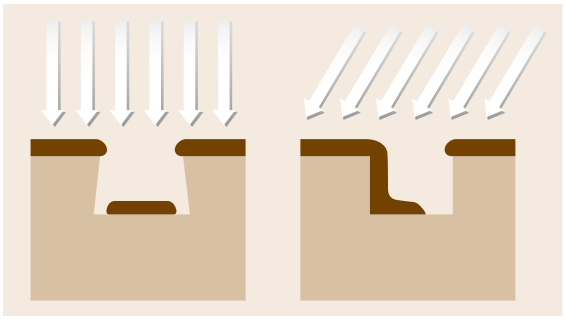

Fig. 8.8 Shadow effects observed in evaporated films. *Arrows* show the trajectory of the material atoms being deposited

sections, some microfabrication techniques utilize these effects to pattern the deposited layer. One way to improve the step coverage is by rotating and/or heating the wafers during deposition.

In sputtering, a target of the material to be deposited is bombarded with high-energy inert ions (usually argon). The outcome of the bombardment is that individual atoms or clusters are removed from the surface and ejected towards the wafer. The physical nature of this process allows its use with virtually any existing material. Examples of interesting materials for microfabrication that are frequently sputtered include metals, dielectrics, alloys (such as shape memory alloys), and all kinds of compounds (for example, piezoelectric lead zirconate titanate (PZT)). The inert ions bombarding the target are produced in direct-current (DC) or RF plasma. In a simple parallel-plate system the top electrode is the target and the wafers are placed horizontally on top of the bottom electrode. In spite of its lower deposition rate, step coverage in sputtering is much better than in evaporation. However, the films obtained with this deposition process are nonconformal. Figure 8.9 illustrates successive sputtering profiles in a trench.

Both evaporation and sputtering systems are often able to deposit more than one material simultaneously or sequentially. This capability is very useful to obtain alloys and multilayer films (e.g., multilayer magnetic recording heads are sputtered). For certain low-reactivity metals such as Au and Pt the previous deposition of a thin layer of another metal is needed to improve adhesion. Ti and Cr are two frequently used adhesion promoters. Stress in evaporated or sputtered layers is typically tensile. The deposition rates are much higher than for most CVD techniques. However, due to stress accumulation and cracking, thickness beyond 2 μm is rarely deposited with these processes.

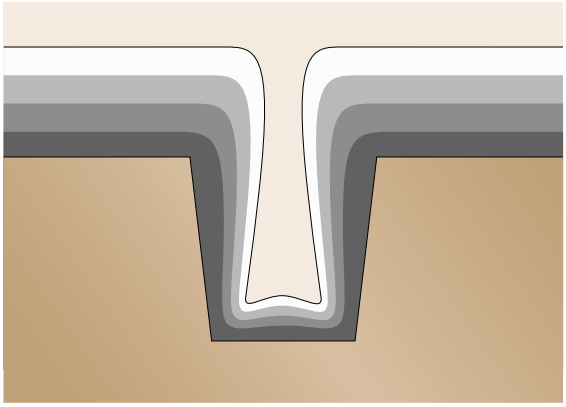

Fig. 8.9 Typical cross section evolution of a trench while being filled with sputter deposition

For thicker deposition a technique described in the next section is sometimes used.

Electroplating

Electroplating (or electrodeposition) is a process typically used to obtain thick (tens of μm) metal structures. The sample to be electroplated is introduced into a solution containing a reducible form of the ion of the desired metal and is maintained at a negative potential (cathode) relative to a counterelectrode (anode). The ions are reduced at the sample surface and the insoluble metal atoms are incorporated into the surface. As an example, copper electrodeposition is frequently done in copper sulfide-based solutions. The reaction taking place at the surface is $Cu^{2+} + 2e^- \rightarrow Cu_{(s)}$. Recommended current densities for electrodeposition processes are on the order of 5–100 mA/cm^2.

As can be deduced from the process mechanism, the surface to be electroplated has to be electrically conductive, and preferably of the same material as the deposited one if good adhesion is desired. In order to electrodeposit metals on top of an insulator (the most frequent case) a thin film of the same metal, called the seed layer, is previously deposited on the surface. Masking of the seed layer with a resist permits selective electroplating of the patterned areas. Figure 8.10 illustrates a typical sequence of the steps required to obtain isolated metal structures.

Pulsed Laser and Atomic Layer Deposition

Pulsed laser and atomic layer deposition techniques have attracted a considerable amount of attention recently. These two techniques offer several unique advantages compared with other thin-film deposition

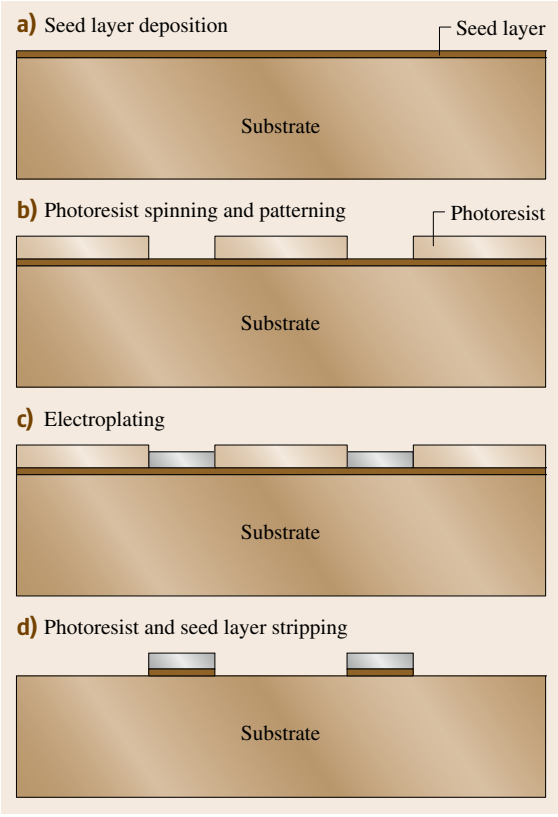

Fig. 8.10a–d Formation of isolated metal structures by electroplating through a mask: **(a)** seed layer deposition, **(b)** photoresist spinning and patterning, **(c)** electroplating, and **(d)** photoresist and seed layer stripping

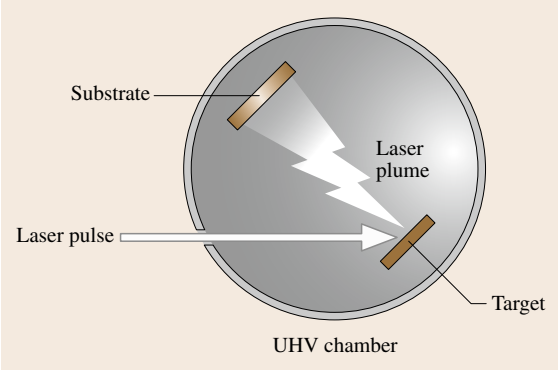

Fig. 8.11 A typical PLD deposition setup

methods that are particularly useful for next-generation nanoscale device fabrication. Pulsed laser deposition (PLD) is a simple technique that uses an intense (1 GW within 25 ns) UV laser (e.g., a KrF excimer) to ablate a target material [8.6]. Plasma is subsequently formed from the target and is deposited on the substrate. Multitarget systems with Auger and reflection high-energy electron diffraction (RHEED) spectroscopes are commercially available. Figure 8.11 shows a typical PLD deposition setup. The main advantages of the PLD are its simplicity and ability to deposit complex materials with preserved stoichiometry (so-called stoichiometry transfer). In addition, fine control over film thickness is also possible by controlling the number of pulses. The stoichiometry-transfer property of the PLD allows many complex targets such as ferroelectrics, superconductors, and magnetostrictives to be deposited. Other deposited materials include oxides, carbides, polymers, and metallic systems (e.g., FeNdB).

Atomic layer deposition (ALD) is a gas-phase self-limiting deposition method capable of depositing atomic layer thin films with excellent large-area uniformity and conformality [8.7]. It enables simple and accurate control over film composition and thickness at the atomic layer level (typical growth rates of a few Å/cycle). Although most of the attention recently has been directed towards depositing high-k dielectric materials (Al_2O_3, and HfO_2) for next-generation complementary metal–oxide–semiconductor (CMOS) electronics, other materials can also be deposited. These include transition metals (Cu, Co, Fe, and Ni), metal oxides, sulfides, nitrides, and fluorides. Atomic-level control over film thickness and composition are also attractive features for applications in MEMS such as conformal three-dimensional (3-D) packaging and air-gap structures. ALD is a modification of the CVD process and is based on two or more vapor-phase reactants that are introduced into the deposition chamber in a sequential manner. One growth cycle consists of four steps. First, a precursor vapor is introduced into the chamber, resulting in the deposition of a self-limiting monolayer on the surface of the substrate. Then, the extra unreacted vapor is pumped out and a vapor dose of a second reactant is introduced. This reacts with the precursor on the surface in a self-limiting fashion. Finally, the extra unreacted vapor is pumped out and the cycle is repeated.

8.1.3 Etching and Substrate Removal

Thin-film and bulk substrate etching is another fabrication step that is of fundamental importance to both VLSI processes and micro/nanofabrication. In the VLSI area, various conducting and dielectric thin films deposited for passivation or masking purposes need to be removed

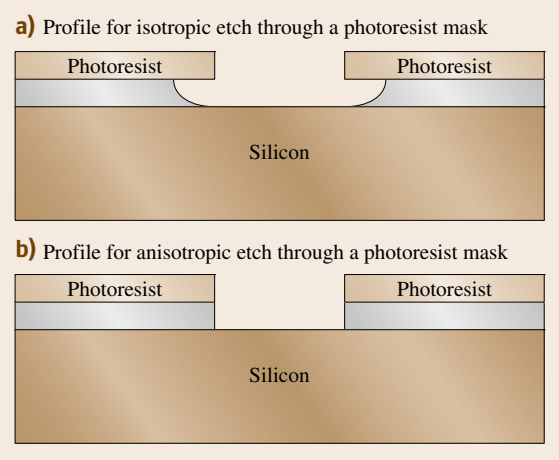

Fig. 8.12a,b Profile for (a) isotropic and (b) anisotropic etching through a photoresist mask

at some point or another. In micro/nanofabrication, in addition to thin-film etching, very often the substrate (silicon, glass, GaAs, etc.) also needs to be removed in order to create various mechanical micro/nanostructures (beams, plates, etc.). Two important figures of merit for any etching process are selectivity and directionality. Selectivity is the degree to which the etchant can differentiate between the masking layer and the layer to be etched. Directionality has to do with the etch profile under the mask. In an isotropic etch, the etchant attacks the material in all directions at the same rate, hence creating a semicircular profile under the mask (Fig. 8.12a). In contrast, in an anisotropic etch, the dissolution rate depends on specific directions and one can obtain straight side-walls or other noncircular profiles (Fig. 8.12b). One can also divide the various etching techniques into wet and dry categories. In this chapter, we will use this classification and discuss different wet etchants first followed by dry etching techniques used most often in the micro/nanofabrication.

Wet Etching

Historically, wet etching techniques preceded the dry ones. These still constitute an important group of etchants for micro/nanofabrication in spite of their less frequent application in the VLSI processes. Wet etchants are by and large isotropic and show superior selectivity to the masking layer as compared with various dry techniques. In addition, due to the lateral undercut, the minimum feature size achievable with wet etchants is limited to $> 3\,\mu m$. Silicon dioxide is commonly etched in dilute (6 : 1, 10 : 1, or 20 : 1 by volume) or buffered HF (BHF: $HF + NH_4F$) solutions (etch rate of $\approx 1000\,Å/min$ in BHF). Photoresist and silicon nitride are the two most common masking materials for the wet oxide etch. The wet etchant for silicon nitride is hot (140–200 °C) phosphoric acid with silicon oxide as the masking material. Nitride wet etch is not very common (except for blanket etch) due to the masking difficulty and nonrepeatable etch rates. Metals can be etched using various combinations of acid and base solutions. There are also many commercially available etchant formulations for aluminum, chromium, and gold which can easily be used. A comprehensive table of various metal etchants can be found in [8.8].

Anisotropic and isotropic wet etching of crystalline (silicon and gallium arsenide) and noncrystalline (glass) substrates is an important topic in micro/nanofabrication [8.9–12]. In particular, the realization of the possibility of anisotropic wet etching of silicon is considered to mark the beginning of the micromachining and MEMS discipline. Isotropic etching of silicon using $HF/HNO_3/CH_3COOH$ (various different formulations have been used) dates back to the 1950s and is still frequently used to thin down the silicon wafer. The etch mechanism for this combination has been elucidated and is as follows: HNO_3 is used to oxidize the silicon, which is subsequently dissolved away in the HF. The acetic acid is used to prevent the dissociation of HNO_3 (the etch works as well without the acetic acid). For short etch times, silicon dioxide can be used as the masking material; however, one needs to use silicon nitride if a longer etch time is desired. This etch also shows dopant selectivity, with the etch rate dropping at lower doping concentrations ($< 10^{17}\,cm^{-3}$ n- or p-type). Although this effect can potentially be used as an etch-stop mechanism in order to fabricate microstructures, the difficulty in masking has prevented widespread application of this approach. Glass can also be isotropically etched using the HF/HNO_3 combination with the etch surfaces showing considerable roughness. This has been extensively used in fabricating microfluidic components (mainly channels). Although Cr/Au is usually used as the masking layer, long etch times require a more robust mask (bonded silicon has been used for this purpose).

Silicon anisotropic wet etch constitutes an important technique in bulk micromachining. The three most important silicon etchants in this category are potassium hydroxide (KOH), ethylenediamine pyrochatechol (EDP), and tetramethyl ammonium hydroxide (TMAH). These are all anisotropic etchants which attack silicon along preferred crystallographic direc-

tions. In addition, they all show marked reduction of the etch rate in heavily ($> 5\times10^{19}\,\mathrm{cm}^{-3}$) boron-doped ($p^{++}$) regions. The chemistry behind the action of these etchants is not yet very clear but it seems that silicon atom oxidation at the surface and its reaction with hydroxyl ions (OH^-) is responsible for the formation of a soluble silicon complex ($SiO_2(OH)^{2-}$). The etch rate depends on the concentration and temperature and is usually around 1 μm/min at temperatures of 85–115 °C. Common masking materials for anisotropic wet etchants are silicon dioxide and nitride, with the latter being superior for longer etch times. The crystallographic plane which shows the slowest etch rate is the (111) plane. Although the lower atomic concentration along these planes has been speculated to be the reason for this phenomena, the evidence is inconclusive and other factors must be included to account for this remarkable etch-stop property. The anisotropic behavior of these etchants with respect to the (111) planes has been extensively used to create beams, membranes, and other mechanical and structural components. Figure 8.13 shows the typical cross sections of (100) and (110) silicon wafers etched with an anisotropic wet etchant. As can be seen, the (111) slow planes are exposed in both situations, one creating 54.7° sloped side-walls in the (100) wafer and the other creating vertical side-walls in the (110) wafer. Depending on the dimensions of the mask opening, a V-groove or a trapezoidal trench is formed in the (100) wafer. A large enough opening will allow the silicon to be etched all

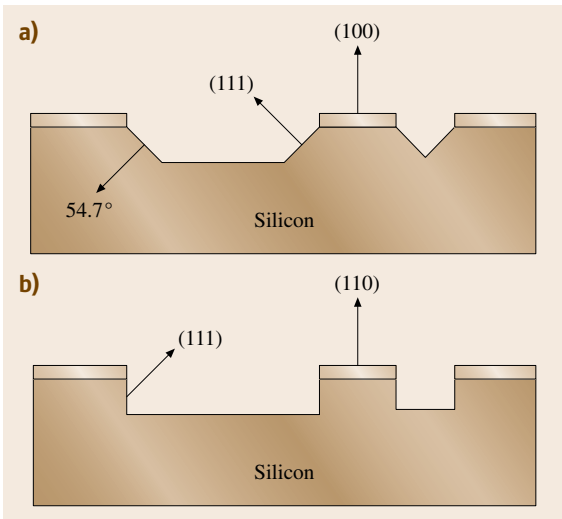

Fig. 8.13a,b Anisotropic etch profiles for: **(a)** (100) and **(b)** (110) silicon wafers

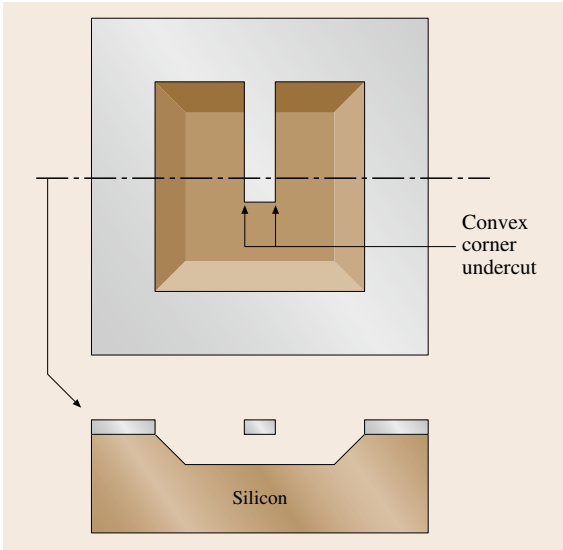

Fig. 8.14 Top view and cross section of a dielectric cantilever beam fabricated using convex corner undercut

the way through the wafer, thus creating a thin dielectric membrane on the other side. It should be mentioned that exposed convex corners have a higher etch rate than concave ones, resulting in an undercut which can be used to create dielectric (e.g., nitride) cantilever beams. Figure 8.14 shows a cantilever beam fabricated using the convex corner undercut on a (100) wafer.

The three above-mentioned etchants show different directional and dopant selectivities. KOH has the best (111) selectivity (400/1), followed by TMAH and EDP. However, EDP has the highest selectivity with respect to deep boron diffusion regions. Safety and CMOS compatibility are other important criteria for choosing a particular anisotropic etchant. Among the three mentioned etchants TMAH is the most benign, whereas EDP is extremely corrosive and carcinogenic. Silicon can be dissolved in TMAH in order to improve its selectivity with respect to aluminum. This property has made TMAH very appealing for post-CMOS micromachining where aluminum lines have to be protected. Finally, it should be mentioned that one can modulate the etch rate using a reversed-biased p–n junction (electrochemical etch stop). Figure 8.15 shows the setup commonly used to perform electrochemical etching. The silicon wafer under etch consists of an n-epi region on a p-type substrate. Upon the application of a reverse-bias voltage to the structure (p-substrate is in contact with the solution and n-epi is protected using a watertight fixture), the p-substrate is etched away. When the n-epi

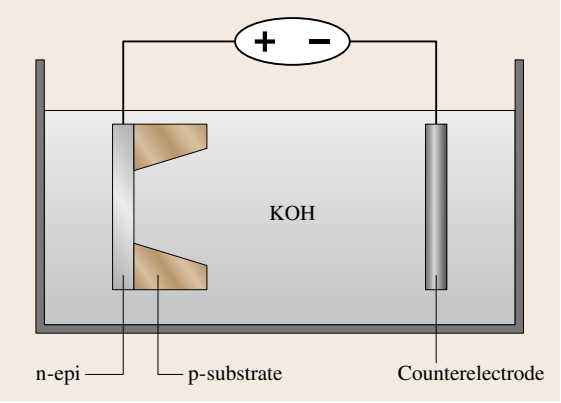

Fig. 8.15 Electrochemical etch setup

regions are exposed to the solution an oxide passivation layer is formed and etching is stopped. This technique can be used to fabricate single-crystalline silicon membranes for pressure sensors and other mechanical transducers.

Dry Etching

Most of the dry etching techniques are plasma based. They have several advantages when compared with wet etching. These include smaller undercut (allowing smaller lines to be patterned) and higher anisotropy (allowing high-aspect-ratio vertical structures). However, the selectivity of dry etching techniques is lower than that of wet etchants, and one must take into account the finite etch rate of the masking materials. The three basic dry etching techniques, namely high-pressure plasma etching, reactive-ion etching (RIE), and ion milling, utilize different mechanisms to obtain directionality.

Ion milling is a purely physical process which utilizes accelerated inert ions (e.g., Ar^+) striking perpendicular to the surface to remove the material ($p \approx 10^{-4}$–10^{-3} Torr) (Fig. 8.16a). The main characteristics of this technique are very low etch rates (in the order of a few nm/min) and poor selectivity (close to 1 : 1 for most materials); hence it is generally used to etch very thin layers. In high-pressure (10^{-1}–5 Torr) plasma etchers highly reactive species are created that

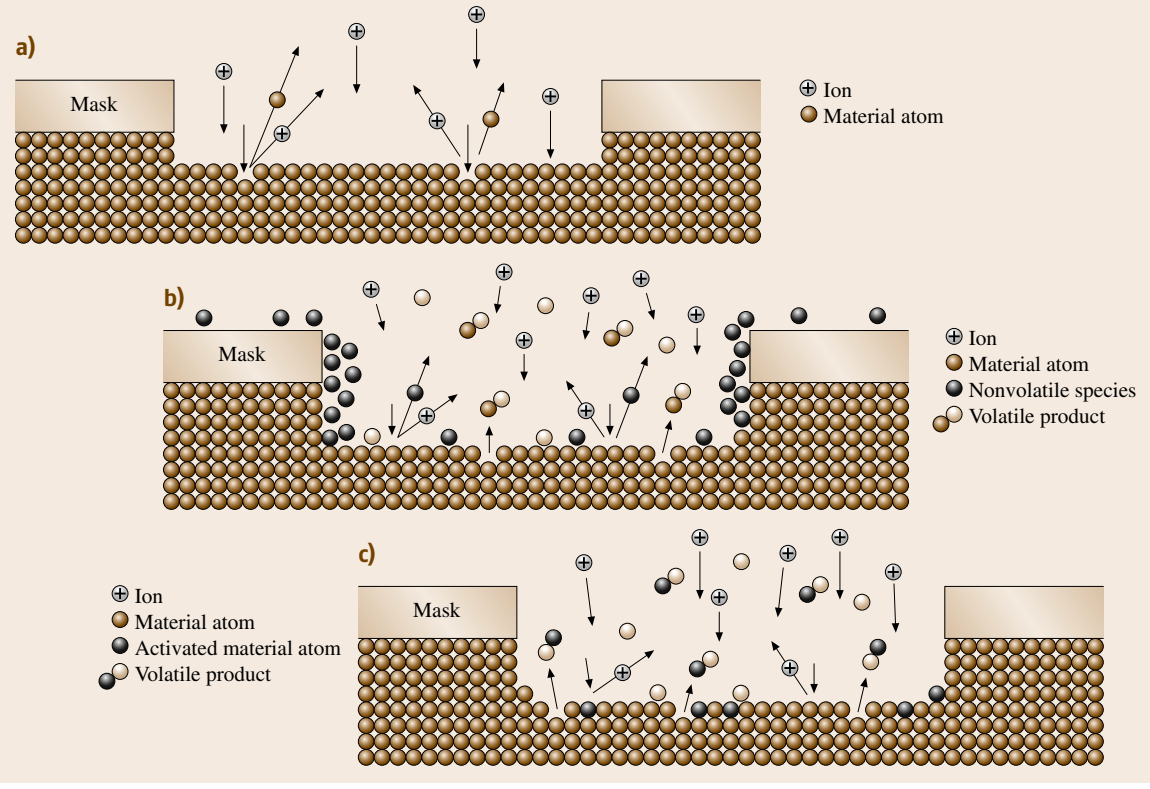

Fig. 8.16a–c Simplified representation of etching mechanisms for: **(a)** ion milling, **(b)** high-pressure plasma etching, and **(c)** RIE

react with the material to be etched. The products of the reaction are volatile so that they diffuse away and new material is exposed to the reactive species. Directionality can be achieved, if desired, with the side-wall passivation technique (Fig. 8.16b). In this technique nonvolatile species produced in the chamber deposit on and passivate the surfaces. The deposit can only be removed by physical collision with incident ions. Because the movement of the ions has a vertical directionality the deposit is removed mainly on horizontal surfaces, while vertical walls remain passivated. In this fashion, the vertical etch rate becomes much higher than the lateral one.

RIE etching, also called ion-assisted etching, is a combination of physical and chemical processes. In this technique the reactive species react with the material only when the surfaces are *activated* by the collision of incident ions from the plasma (e.g., by breaking bonds at the surface). As in the previous technique, the directionality of the ion's velocity produces much more collisions on the horizontal surfaces than on the walls, thus generating faster etching rates in the vertical direction (Fig. 8.16c). To increase the etch anisotropy further, in some cases side-wall passivation methods are also used. An interesting case is the deep reactive-ion etching (DRIE) technique, capable of achieving aspect ratios of 30 : 1 and silicon etching rates of 2–3 μm/min (through wafer etch is possible). In this technique, the passivation deposition and etching steps are performed sequentially in a two-step cycle, as shown in Fig. 8.17. In commercial silicon DRIE etchers SF_6/Ar is typically used for the etching step and a combination of Ar and a fluoropolymer (nCF_2) for the passivation step. A Teflon-like polymer about 50 nm thick is deposited during the latter step, covering only the side-walls (Ar^+ ion bombardment removes the Teflon on the horizontal surfaces). Due to the cyclic nature of this process, the side-walls of the etched features show a periodic *wave-shaped* roughness in the range of 50–400 nm. More recently, *Aimi* et al., reported on a similar method for deep etching of titanium. In this case titanium oxide was used as a side-wall passivation layer [8.13].

Dry etching can also be performed in nonplasma equipment if the etching gases are reactive enough. The so-called vapor-phase etching (VPE) processes can be carried out in a simple chamber with gas feeding and pumping capabilities. Two examples of VPE are xenon difluoride (XeF_2) etching of silicon and HF vapor etching of silicon dioxide. Due to its isotropic nature, these processes are typically used for etching sacrificial layers and releasing structures while avoiding stiction problems (Sects. 8.2.1 and 8.2.2).

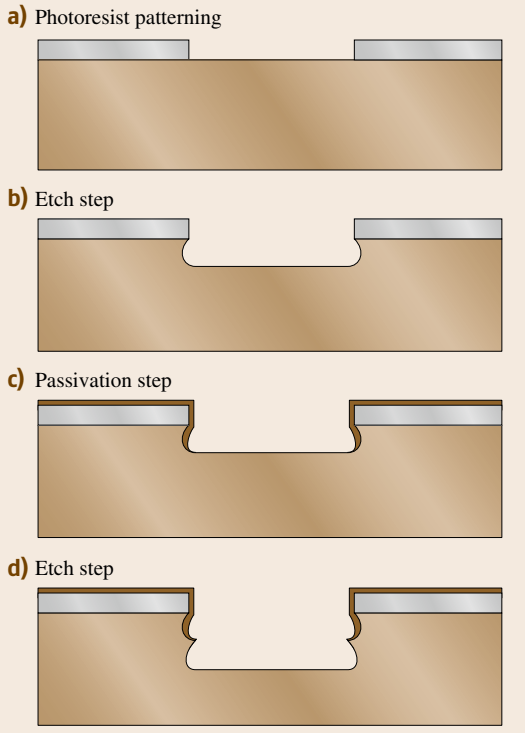

Fig. 8.17a–d DRIE cyclic process: (a) photoresist patterning, (b) etch step, (c) passivation step, and (d) etch step

Most important materials can be etched with the aforementioned techniques, and for each material a variety of chemistries are available. Table 8.1 lists some of the most common materials along with selected etch

Table 8.1 Typical dry etch chemistries

Si	CF_4/O_2, CF_2Cl_2, CF_3Cl, $SF_6/O_2/Cl_2$, $Cl_2/H_2/C_2F_6/CCl_4$, C_2ClF_5/O_2, Br_2, SiF_4/O_2, NF_3, ClF_3, CCl_4, $C_3Cl_3F_5$, C_2ClF_5/SF_6, C_2F_6/CF_3Cl, CF_3Cl/Br_2
SiO_2	CF_4/H_2, C_2F_6, C_3F_8, CHF_3/O_2
Si_3N_4	$CF_4/O_2/H_2$, C_2F_6, C_3F_8, CHF_3
Organics	O_2, CF_4/O_2, SF_6/O_2
Al	BCl_3, BCl_3/Cl_2, $CCl_4/Cl_2/BCl_3$, $SiCl_4/Cl_2$
Silicides	CF_4/O_2, NF_3, SF_6/Cl_2, CF_4/Cl_2
Refractories	CF_4/O_2, NF_3/H_2, SF_6/O_2
GaAs	BCl_3/Ar, $Cl_2/O_2/H_2$, CCl_2F_2/O_2/Ar/He, H_2, CH_4/H_2, $CClH_3/H_2$
InP	CH_4/H_2, C_2H_6/H_2, Cl_2/Ar
Au	$C_2Cl_2F_4$, Cl_2, $CClF_3$

recipes [8.14]. For each chemistry the etch rate, directionality, and selectivity with respect to the mask materials depend on parameters such as the flow rates of the gases entering the chamber, the working pressure, and the RF power applied to the plasma.

8.1.4 Substrate Bonding

Substrate (wafer) bonding (silicon–silicon, silicon–glass, and glass–glass) is among the most important fabrication techniques in microsystem technology [8.15, 16]. It is frequently used to fabricate complex 3-D structures both as a functional unit and as a part of the final microsystem package and encapsulation. The two most important bonding techniques are silicon–silicon fusion (or silicon direct bonding) and silicon–glass electrostatic (or anodic) bonding. In addition to these techniques, several other alternative methods which utilize an intermediate layer (eutectic, adhesive, and glass frit) have also been investigated. All these techniques can be used to bond the substrates at the wafer level. In this section we will only discuss wafer-level techniques and will not treat device-level bonding methods (e.g., e-beam and laser welding).

Silicon Direct Bonding

Direct silicon or fusion bonding is used in the fabrication of micromechanical devices and silicon-on-insulator (SOI) substrates. Although it is mostly used to bond two silicon wafers with or without an oxide layer, it has also been used to bond different semiconductors such as GaAs and InP [8.16]. One main requirement for a successful bond is sufficient planarity (< 10 Å surface roughness and $< 5\,\mu$m bow across a 4 inch wafer) and cleanliness of the surfaces. In addition, thermal expansion mismatch also needs to be considered if bonding of two dissimilar materials is contemplated. The bonding procedure is as follows: the silicon or oxide-coated silicon wafers are first thoroughly cleaned. Subsequently the surfaces are hydrated (activated) in HF or boiling nitric acid (Radio Corporation of America (RCA) clean also works). This renders the surfaces hydrophilic by creating an abundance of hydroxyl ions. Then the substrates are brought together in close proximity (starting from the center to avoid void formation). The close approximation of the bonding surfaces allows the short-range attractive van der Waals forces to bring the surfaces into intimate contact on the atomic scale. Following this step, hydrogen bonds between the two hydroxyl-coated silicon wafers bond the substrates together. These steps can be performed at room temperature; however, in order to increase the bond strength, a high-temperature (800–1200 °C) anneal is usually required. A major advantage of silicon fusion bonding is the thermal matching of the substrates.

Anodic Bonding

Silicon–glass anodic (electrostatic) bonding is another major substrate joining technique which has been extensively used for microsensor packaging and device fabrication. The main advantage of this technique is its lower bonding temperature, which is around 300–400 °C. Figure 8.18 shows the bonding setup. A glass wafer (usually Pyrex 7740 because of thermal expansion match to silicon) is placed on top of a silicon wafer and the sandwich is heated to 300–400 °C. Subsequently, a voltage of ≈ 1000 V is applied to the glass–silicon sandwich with the glass connected to the cathode. The bond starts immediately after the application of the voltage and spreads outward from the cathode contact point. The bond can be observed visually as a dark-grayish front which expands across the wafer.

The bonding mechanism is as follows. During the heating period, glass sodium ions move toward the cathode and create a depletion layer at the silicon–glass interface. A strong electrostatic force is therefore created at the interface, which pulls the substrates into intimate contact. The exact chemical reaction responsible for anodic bonding is not yet clear, but covalent silicon–oxygen bonds at the interface seem to be responsible for the bond. Silicon–silicon anodic bonding using sputtered or evaporated glass interlayer is also possible.

Bonding with Intermediate Layers

Various other wafer bonding techniques utilizing an intermediate layer have also been investigated [8.16]. Among the most important ones are adhesive, eutectic, and glass frit bonds. Adhesive bonding using a poly-

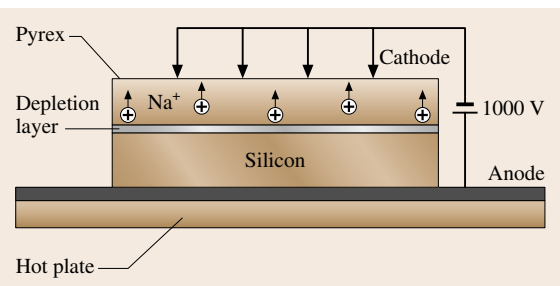

Fig. 8.18 Glass–silicon anodic bonding setup

mer (e.g., polyimides, epoxies, thermoplastic adhesives, and photoresists) in between the wafers has been used to join different wafer substrates [8.17]. Complete curing (in an oven or using dielectric heating) of the polymer before or during the bonding process prevents subsequent solvent outgassing and void formation. Although reasonably high bonding strengths can be obtained, these bonds are nonhermetic and unstable over a period of time.

In eutectic bonding process, gold-coated silicon wafers are bonded together at temperatures greater than the silicon–gold eutectic point (363 °C, 2.85% silicon and 97.1% Au) [8.18]. This process can achieve high bonding strength and good stability at relatively low temperatures. For good bond uniformity silicon dioxide must be removed from the silicon surface prior to the deposition of the gold. In addition, all organic contaminants on the gold surface must be removed (using UV light) prior to the bond. Pressure must also be applied in order to achieve a better contact. Although eutectic bonding can be accomplished at low temperatures, achieving uniformity over large areas has proven to be challenging.

Glass frit can also be used as an interlayer in substrate bonding. In this technique, first a thin layer of glass is deposited and preglazed. The glass-coated substrates are then brought into contact and the sandwich is heated to above the glass melting temperature (typically $< 600\,°C$). As for the eutectic process, pressure must be applied for adequate contact [8.19].

8.2 MEMS Fabrication Techniques

In this section, we will discuss various important MEMS fabrication techniques commonly used to build various microdevices (microsensors and microactuators) [8.9–12]. The dimensional spectrum of the microstructures that can be fabricated using these techniques spans from 1 mm to 1 μm. As mentioned in the introduction, we will mostly emphasize the more important techniques and will not discuss specialized methods.

8.2.1 Bulk Micromachining

Bulk micromachining is the oldest MEMS technology and hence probably one of the more mature ones [8.20]. It is currently by far the most commercially successful one, helping to manufacture devices such as pressure sensors and inkjet printheads. Although there are many different variations, the basic concept behind bulk micromachining is selective removal of the substrate (silicon, glass, GaAs, etc.). This allows the creation of various micromechanical components such as beams, plates, and membranes which can be used to fabricate a variety of sensors and actuators. The most important microfabrication techniques used in bulk micromachining are wet and dry etching and substrate bonding. Although one can use various criteria to categorize bulk micromachining techniques, we will use a historical timeline for this purpose. Starting with the more traditional wet etching techniques, we will proceed to discuss the more recent ones using deep RIE and wafer bonding.

Bulk Micromachining Using Wet Etch and Wafer Bonding

The use of anisotropic wet etchants to remove silicon can be marked as the beginning of the micromachining era. Back-side etch was used to create movable structures such as beams, membranes, and plates (Fig. 8.19). Initially, etching was timed in order to create a specified thickness. However, this technique proved to be inadequate for the creation of thin structures ($< 20\,\mu m$). Subsequent use of various etch-stop techniques allowed the creation of thinner membranes in a more controlled fashion. As was mentioned in *High-Aspect Ratio Micromachining*, heavily boron-doped regions and electrochemical bias can be used to slow down the etch process drastically and hence create controllable thickness microstructures. Figure 8.20a,b shows the cross section of two piezoresistive pressure sensors fabricated using electrochemical and p^{++} etch-stop techniques. The use of the p^{++} method requires epitaxial growth

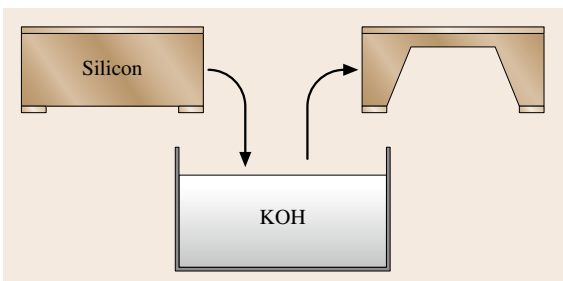

Fig. 8.19 Wet anisotropic silicon back-side etch

of a lightly doped region on top of a p^{++} etch-stop layer. This layer is subsequently used for the placement of piezoresistors. However, if no active component is required one can simply use the p^{++} region to create a thin membrane (Fig. 8.20c).

The p^{++} etch-stop technique can also be used to create isolated thin silicon structures through the dissolution of the entire lightly doped region [8.21]. This technique was successfully used to fabricate silicon recording and stimulating electrodes for biomedical applications. Figure 8.21 shows the cross section of such a process which relies on deep (15–20 μm) and shallow boron (2–5 μm) diffusion steps to create microelectrodes with flexible connecting ribbon cables. An extension of this process which uses a combination of p^{++} etch-stop layers and silicon–glass anodic bonding has also been developed. This process is commonly known as the dissolved wafer process and has been used to fabricate a variety of microsensors and microactuators [8.22]. Figure 8.22 shows

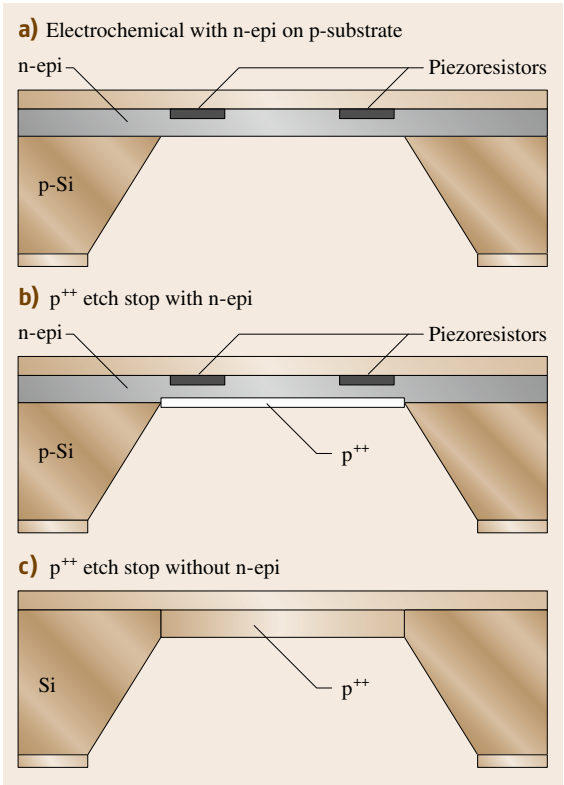

Fig. 8.20a–c Wet micromachining etch-stop techniques: **(a)** electrochemical with n-epi on p-substrate, **(b)** p^{++} etch stop with n-epi, and **(c)** p^{++} etch stop without n-epi

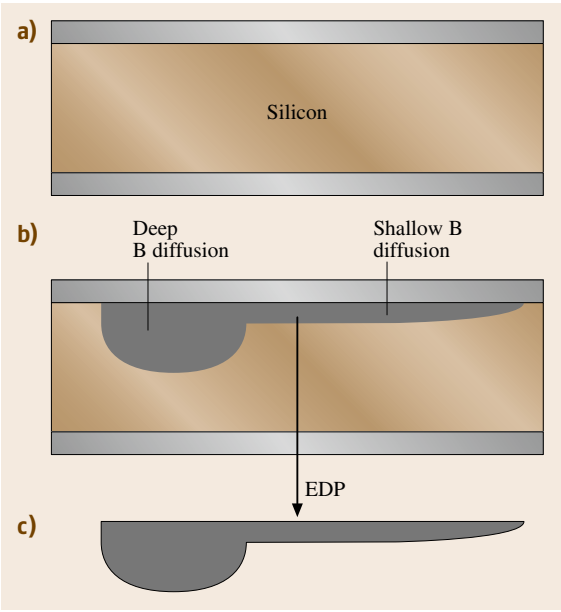

Fig. 8.21a–c Free-standing microstructure fabrication using deep and shallow boron diffusion and EDP release **(a)** silicon wafer, **(b)** deep and shallow boron diffusion, and **(c)** EDP etch

the cross section of this process. Figure 8.23 shows a scanning electron microscopy (SEM) photograph of a microaccelerometer fabricated using the dissolved wafer process.

It is also possible to merge wet bulk micromachining and microelectronics fabrication processes to build micromechanical components on the same substrate as the integrated circuits (CMOS, bipolar, or biopolar complementary metal oxide semiconductor (BiCMOS)) [8.23]. This is very appealing since it allows the integration of interface and signal-processing circuitry with MEMS structures on a single chip. However, important fabrication issues such as process compatibility and yield have to be carefully considered. Among the most popular techniques in this category is postprocessing of CMOS integrated circuits by front-side etching in TMAH solutions. As was mentioned previously, silicon-rich TMAH does not attack aluminum and therefore can be used to undercut microstructures in an already processed CMOS chip. Figure 8.24 shows a schematic of such a process in which a front-side wet etch and electrochemical etch stop are used to produce suspended beams. This technique has been extensively used to fabricate a variety of microsensors (e.g., humidity, gas, chemical, and

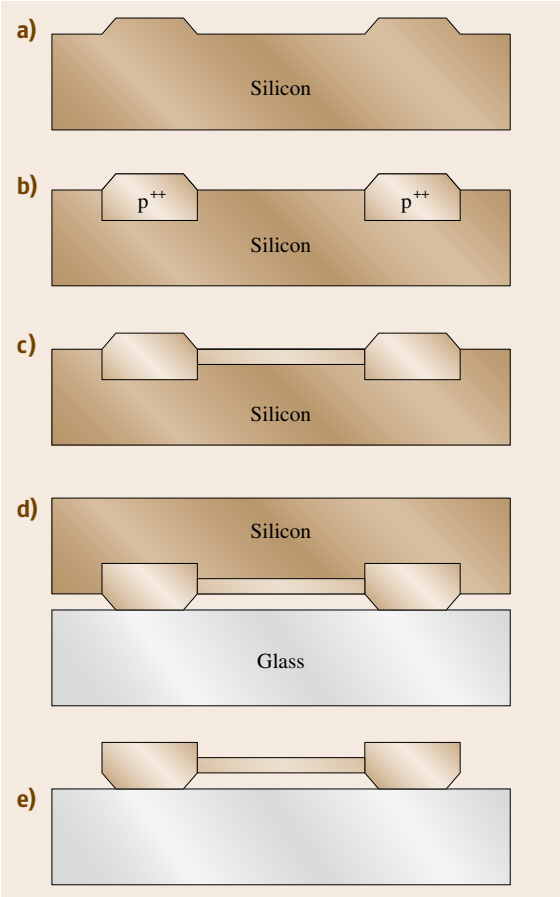

Fig. 8.22a–e Dissolved wafer process sequence: **(a)** KOH etch, **(b)** deep B diffusion, **(c)** shallow B diffusion, **(d)** silicon–glass anodic bond, and **(e)** release in EDP

pressure). Figure 8.25 shows a photograph of a post-CMOS-processed chemical sensor.

Bulk Micromachining Using Dry Etch

Bulk silicon micromachining using dry etching is a very attractive alternative to the wet techniques described in the previous section. These techniques were developed during the mid 1990s subsequent to successful efforts geared towards the development of processes for anisotropic dry silicon etch. More recent advances in deep silicon RIE and the availability of SOI wafers with a thick top silicon layer have increased the applicability of these techniques. These techniques allow the fabrication of high-aspect-ratio vertical structures in isolation or along with on-chip electronics. Process compatibility with active microelectronics is less of a concern in dry

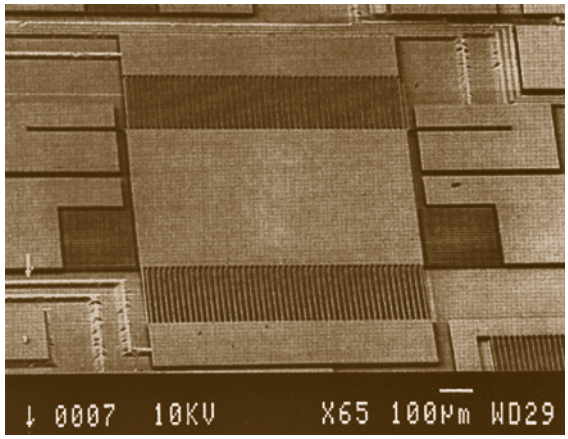

Fig. 8.23 SEM image of a microaccelerometer fabricated using the dissolved wafer process (after [8.22])

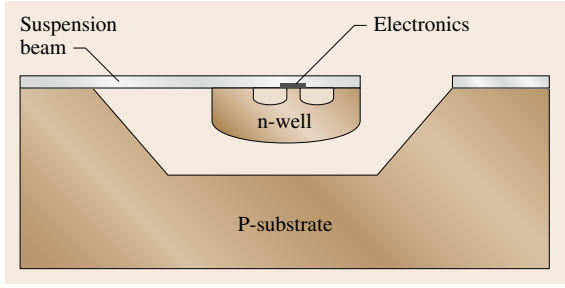

Fig. 8.24 Suspended island created on a prefabricated CMOS chip using front-side wet etch and electrochemical etch stop

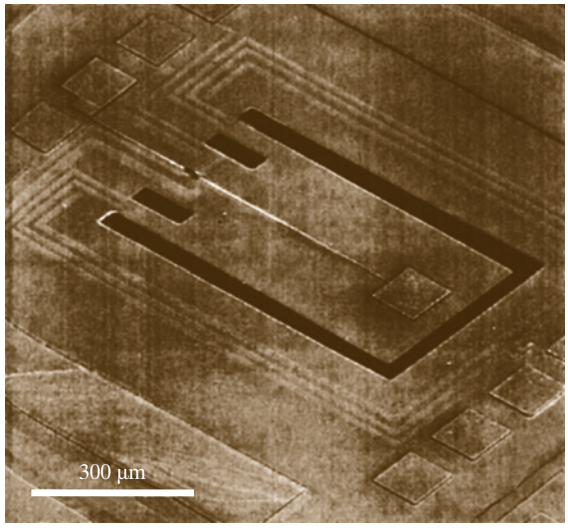

Fig. 8.25 Photograph of a post-CMOS-processed cantilever beam resonator for chemical sensing (after [8.23])

methods since many of them do not damage the circuit or its interconnect.

The simplest dry bulk micromachining technique relies on front-side undercut of microstructures using a XeF_2 vapor-phase etch [8.25]. As was mentioned before, this however, is an isotropic etch and therefore has limited applications. A combination of isotropic/anisotropic dry etch is more useful and can be used to create a variety of interesting structures. Two successful techniques using this combination are single-crystal reactive etching and metallization (SCREAM) [8.26] and post-CMOS dry release using aluminum/silicon dioxide laminate [8.27]. The first technique relies on the combination of isotropic/anisotropic dry etch to create single-crystalline suspended structures. Figure 8.26 shows the cross section of this process. It starts with an anisotropic (Cl_2/BCl_3) silicon etch using an oxide mask (Fig. 8.26b). This is followed by a conformal PECVD oxide deposition (Fig. 8.26c). Subsequently an anisotropic oxide etch is used to remove the oxide at the bottom of the trenches leaving the side-wall oxide intact (Fig. 8.26d). At this stage an isotropic silicon etch (SF_6) is performed, which results in undercut and release of the silicon structures (Fig. 8.26e). Finally, if electrostatic actuation is desired, a metal can be sputtered to cover the top and side-wall of the microstructure and bottom of the cavity formed below it (Fig. 8.26f). Figure 8.27 shows an SEM photograph of a comb-drive actuator fabricated using SCREAM technology.

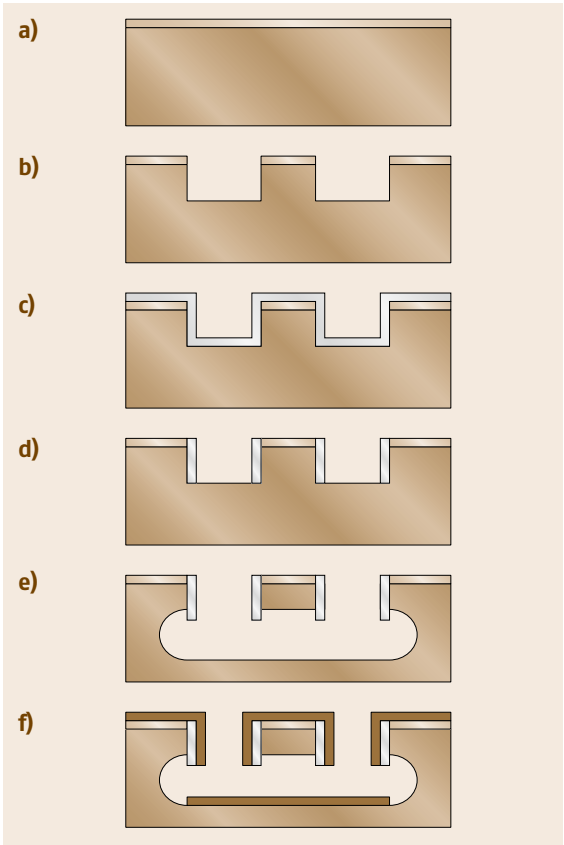

Fig. 8.26a–f Cross section of the SCREAM process **(a)** silicon wafer, **(b)** anisotropic silicon etch, **(c)** conformal passivation, **(d)** anisotropic etching of the passivation (hence protecting the sidewall), **(e)** isotropic silicon etch, and **(f)** metal deposition

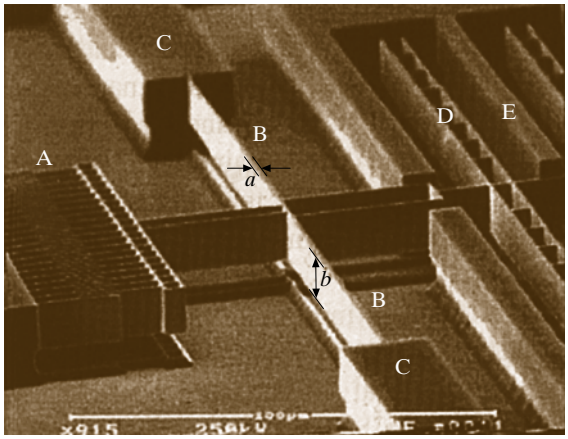

Fig. 8.27 SEM image of a structure fabricated using the SCREAM process: *A* comb-drive actuator, *B* suspended spring, *C* spring support, *D* moving suspended capacitor plate, and *E* fixed capacitor plate (after [8.24])

The second dry release technique relies on the masking capability of aluminum interconnect lines in a CMOS integrated circuit to create suspended microstructures. Figure 8.28 shows a cross section of this process. As can be seen the third level Al of a prefabricated CMOS chip is used as a mask to etch the underlying oxide layers anisotropically all the way to the silicon (CHF_3/O_2) (Fig. 8.28b). This is followed by an anisotropic silicon etch to create a recess in the silicon, which will be used in the final step to facilitate the undercut and release (Fig. 8.28c). Finally, an isotropic silicon etch is used to undercut and release the structures (Fig. 8.28d). Figure 8.29 shows an SEM photograph of a comb-drive actuator fabricated using this technology.

In addition to the methods described above, recent advancements in the development of deep reactive-ion etching of silicon (DRIE) have created new op-

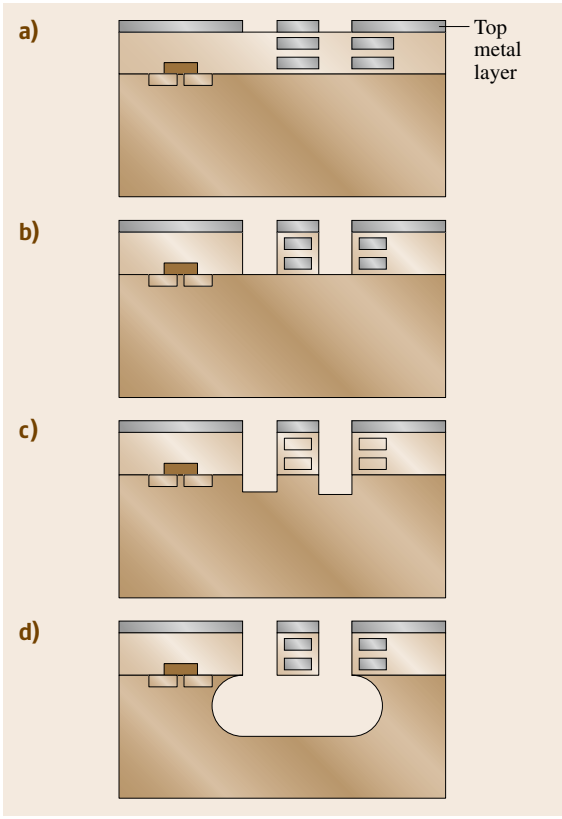

Fig. 8.28a–d Cross section of the process flow for post-CMOS dry microstructure fabrication

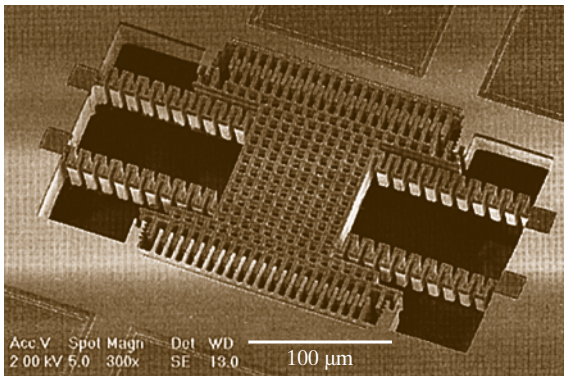

Fig. 8.29 SEM image of a comb-drive actuator fabricated using aluminum-mask post-CMOS dry release (after [8.29])

portunities for dry bulk micromachining techniques (Sect. 8.2.3). One of the most important ones uses thick silicon SOI wafers which are commercially available

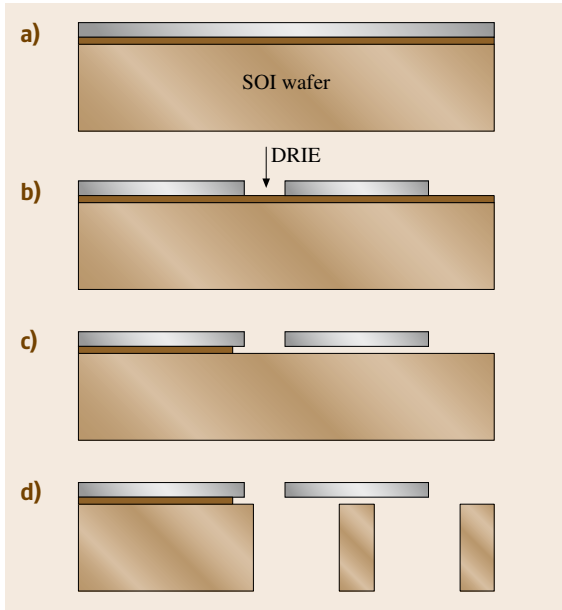

Fig. 8.30a–d DRIE processes using SOI wafers

in various top silicon thicknesses [8.28]. Figure 8.30 shows a cross section of a typical process using DRIE and SOI wafers. The top silicon layer is patterned and etched all the way to the buried oxide (Fig. 8.30b). The oxide is subsequently removed in HF, hence releasing suspended single-crystalline microstructures (Fig. 8.30c). In a modification of this process, the substrate can also be removed from the back-side, allowing easy access from both sides (which allows easier release and prevents stiction) (Fig. 8.30d).

8.2.2 Surface Micromachining

Surface micromachining is another important MEMS microfabrication technique which can be used to create movable microstructures on top of a silicon substrate [8.30]. This technique relies on the deposition of structural thin films on a sacrificial layer which is subsequently etched away, resulting in movable micromechanical structures (beams, membranes, plate, etc.). The main advantage of surface micromachining is that extremely small sizes can be obtained. In addition, it is relatively easy to integrate the micromachined structures with on-chip electronics for increased functionality. However, due to the increased surface nonplanarity with any additional layer, there is a limit to the number of layers that can be deposited. Although one of the earliest reported MEMS structures

was a surface-micromachined resonant gate transistor [8.31], material-related difficulties resulted in the termination of efforts in this area. In the mid 1980s, improvements in the field of thin-film deposition rekindled interest in surface micromachining [8.32]. Later in the same decade polysilicon surface micromachining was introduced which opened the door to the fabrication of a variety of microsensors (accelerometers, gyroscopes, etc.) and microactuators (micromirrors, RF switches, etc.). In this section, we will concentrate on the key process steps involved in surface-micromachining fabrication and the various materials used. In addition, monolithic integration of CMOS with MEMS structures and 3-D surface micromachining are also discussed.

Basic Surface-Micromachining Processes

The basic surface-micromachining process is illustrated in Fig. 8.31. The process begins with a silicon substrate, on top of which a sacrificial layer is grown and patterned (Fig. 8.31a). Subsequently, the structural material is deposited and patterned (Fig. 8.31b). As can be seen the structural material is anchored to the substrate through the openings created in the sacrificial layer during the previous step. Finally, the sacrificial layer is removed, resulting in the release of the microstructures (Fig. 8.32c). In wide structures, it is usually necessary to provide access holes in the structural layer for

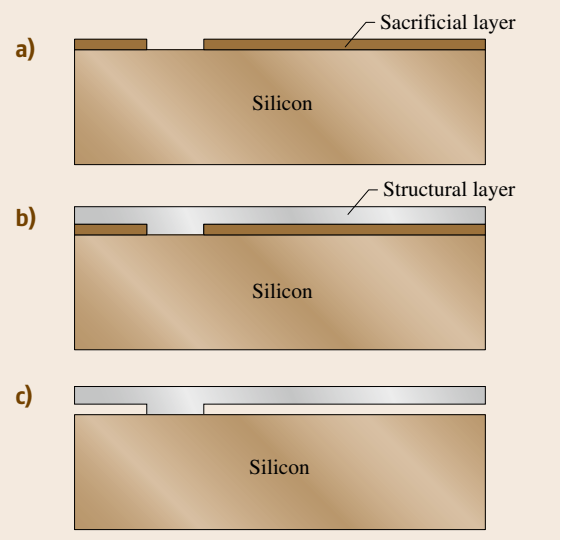

Fig. 8.31a–c Basic surface-micromachining fabrication process **(a)** silicon wafer with patterned sacrificial layer, **(b)** deposition and patterning of the structural layer, and **(c)** removal of the sacrificial layer

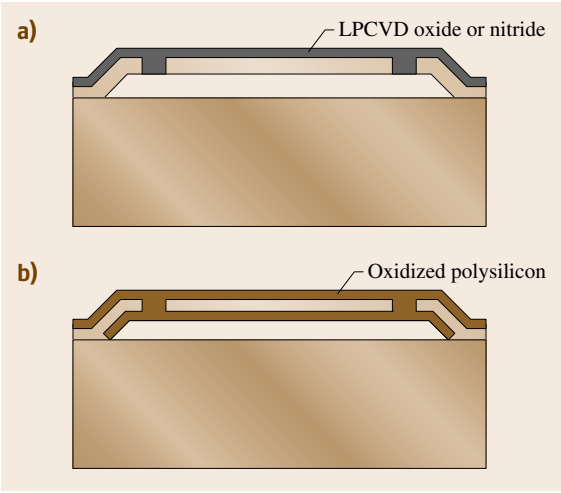

Fig. 8.32a,b Two sealing techniques for cavities created by surface micromachining

fast sacrificial layer removal. It is also possible to seal microcavities created by the surface-micromachining technique [8.11]. This can be done at the wafer level and is a big advantage in applications such as pressure sensors which require a sealed cavity. Figure 8.32 shows two different techniques that can be used for this purpose. In the first technique, following the etching of the sacrificial layer, a LPCVD dielectric layer (oxide or nitride) is deposited to cover and seal the etch holes in the structural material (Fig. 8.33a). Since the LPCVD deposition is performed at reduce pressures, a subatmospheric pillbox microcavity can be created. In the second technique, also called reactive sealing, the polysilicon structural material is oxidized following the sacrificial layer removal (Fig. 8.33b). If access holes are small enough the grown oxide can seal the cavity. Due to the consumption of oxygen during the growth process, in this case also the cavity is subatmospheric.

The most common sacrificial and structural materials are phosphosilicate glass (PSG) and polysilicon, respectively (low-temperature oxide, LTO, is also frequently used as the sacrificial layer). However, there are several other sacrificial/structural combinations that have been used to create a variety of surface-micromachined structures. Important design issues related to the choice of the sacrificial layer are:

1. Quality (pinholes, etc.)
2. Ease of deposition
3. Deposition rate
4. Deposition temperature

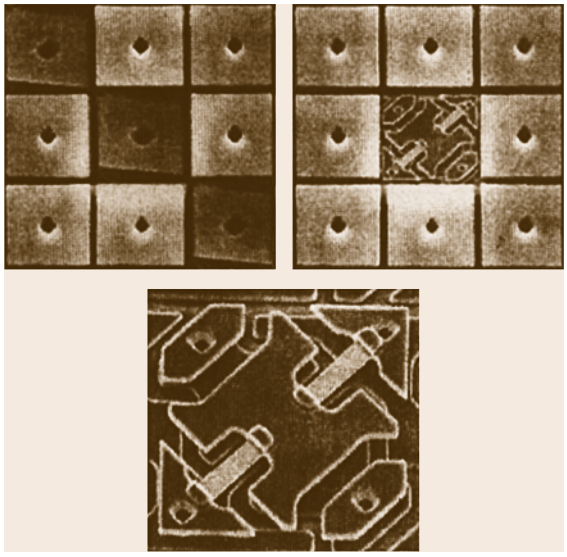

Fig. 8.33 SEM images of the Texas Instrument micromirror array (after [8.30])

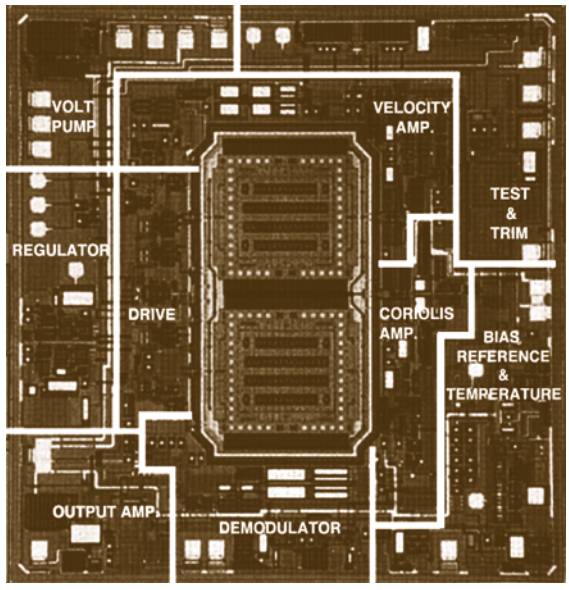

Fig. 8.34 SEM image of the Analog Devices gyroscope (after [8.33])

5. Etch difficulty and selectivity (sacrificial layer etchant should not attack the structural layer)

The particular choice of material for the structural layer depends on the desired properties and specific application. Several important requirements are:

1. Ease of deposition
2. Deposition rate
3. Step coverage
4. Mechanical properties (internal stress, stress gradient, Young's moduli, fracture strength, and internal damping)
5. Etch selectivity
6. Thermal budget and history
7. Electrical conductivity
8. Optical reflectivity

Two examples of commercially available surface-micromachined devices illustrate various successful sacrificial/structural combinations. The Texas Instruments (TI) deformable mirror display (DMD) spatial light modulator uses aluminum as the structural material (good optical reflectivity) and photoresist as the sacrificial layer (easy dry etch and low processing temperatures, allowing easy post-IC integration with CMOS) [8.34] (Fig. 8.33), whereas the Analog Devices microgyroscope uses polysilicon structural material and a PSG sacrificial layer (Fig. 8.34). Two recent additions to the collection of available structural layers are polysilicon–germanium and polygermanium [8.35, 36]. These are intended as substitutes for polysilicon in applications where the high polysilicon deposition temperature (around 600 °C) is prohibitive (e.g., CMOS integration). Unlike in LPCVD of polysilicon, polygermanium (poly-Ge) and polysilicon–germanium (poly-$Si_{1-x}Ge_x$) can be deposited at temperatures as low as 350 °C (poly-Ge deposition temperature is

Table 8.2 Several important surface-micromachined sacrificial–structural combinations

System	Sacrificial layer	Structural layer	Structural layer etchant	Sacrificial layer etchant
1	PSG or LTO	Poly-Si	RIE	Wet or vapor HF
2	Photoresist, polyimide	Metals (Al, Ni, Co, Ni-Fe)	Various metal etchants	Organic solvents, plasma O_2
3	Poly-Si	Nitride	RIE	KOH
4	PSG or LTO	Poly-Ge	H_2O_2 or RCA1	Wet or vapor HF
5	PSG or LTO	Poly-Si-Ge	H_2O_2 or RCA1	Wet or vapor HF

usually lower than that for poly-SiGe). Table 8.2 summarizes important surface-micromachined sacrificial/structural combinations.

An important consideration in the design and processing of surface-micromachined structures is the issue of stiction [8.11, 37, 38]. This can happen during the release step if a wet etchant is used to remove the sacrificial layer or during the device lifetime. The reason for stiction during release is the surface tension of the liquid etchant, which can hold the microstructure down and cause stiction. This usually happens when the structure is compliant and does not possess enough spring constant to overcome the surface tension force of the rinsing liquid (i. e., water). There are several ways one can alleviate the release-related stiction problem. These include:

1. The use of dry or vapor phase etchant
2. The use of solvents with lower surface tension
3. Geometrical modifications
4. CO_2 critical drying
5. Freeze-drying
6. Self-assembled monolayer (SAM) or organic thin-film surface modification

The first technique prevents stiction by not using a wet etchant, although in the case of vapor-phase release, condensation is still possible and can cause some stiction. The second method uses rinsing solvents such as methanol with a lower surface tension than water. This is usually followed by rapid evaporation of the solvent on a hot-plate. However, this technique is not optimum and many structures still stick. The third technique is geometrical, providing dimples in the structural layer in order to reduce the contact surface area and hence reduce the attractive force. The fourth and fifth techniques rely on phase change (in one case CO_2 and the other butyl alcohol) which avoids the liquid phase altogether by directly going to the gas phase. The last technique uses self-assembled monolayers or organic thin films to coat the surfaces with a hydrophobic layer. The stiction that occurs during the operating lifetime of the device (in-use stiction) is due to condensation of moisture on the surfaces, electrostatic charge accumulation, or direct chemical bonding. Surface passivation using self-assembled monolayers or organic thin films can be used to reduce the surface energy and reduce or eliminate capillary forces and direct chemical bonding. These organic coatings also reduce electrostatic forces if a thin layer is applied directly to the semiconductor (without an intervening oxide layer). Commonly used organic coatings include fluorinated fatty acids (TI aluminum micromirrors), silicone polymeric layers (Analog Devices accelerometers), and siloxane self-assembled monolayers.

Surface-Micromachining Integration with Active Electronics

Integration of surface-micromachined structures with on-chip circuitry can increase performance and simplify packaging. However, issues related to process compatibility and yield have to be carefully considered. The two most common techniques are MEMS-first and MEMS-last techniques. In the MEMS-last technique, the integrated circuit is first fabricated and surface-micromachined structures are subsequently built on top of the silicon wafer. An aluminum structural layer with a sacrificial photoresist layer is an attractive combination due to the low thermal budget of the process (TI micromirror array). However, in applications where mechanical properties of Al are not adequate, polysilicon structural material with an LTO or PSG sacrificial layer must be used. Due to the rather high deposition temperature of polysilicon, this combination requires special attention with regard to the thermal budget. For example, aluminum metallization must be avoided and substituted with refractory metals such as tungsten. This can only be achieved at the cost of greater process complexity and lower transistor performance.

The MEMS-first technique alleviates these difficulties by fabricating the microstructures at the very beginning of the process. However, if the microstructures are processed first, they have to be buried in a sealed trench to eliminate the interference of microstructures with subsequent CMOS processes. Figure 8.35 shows a cross section of a MEMS-first fabrication process developed at the Sandia National Laboratory [8.39]. The process starts with shallow anisotropic etching

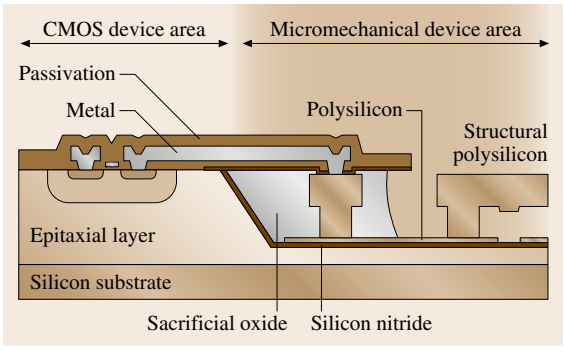

Fig. 8.35 Cross section of the Sandia MEMS-first integrated fabrication process

of trenches in a silicon substrate to accommodate the height of the polysilicon structures fabricated later on. A silicon nitride layer is then deposited to provide isolation at the bottom of the trenches. Next, several layers of polysilicon and sacrificial oxide are deposited and patterned in a standard surface-micromachining process. Subsequently, the trenches are completely filled with sacrificial oxide and the wafers are planarized with chemical–mechanical polishing (this avoids complication in the following lithographic steps). After an annealing step, the trenches are sealed with a nitride cap. At this point, a standard CMOS fabrication process is performed. At the end of the CMOS process the nitride cap is etched and the buried structures released by etching the sacrificial oxide.

Three-Dimensional Microstructures Using Surface Micromachining

Three-dimensional surface microstructures can be fabricated using surface micromachining. The fabrication of hinges for the vertical assembly of MEMS was a major advance towards achieving 3-D microstructures [8.41]. Optical microsystems have greatly benefited from surface-micromachined 3-D structures. These microstructures are used as passive or active components (micromirror, Fresnel lens, optical cavity, etc.) on a silicon optical bench (silicon microphotonics). An example is a Fresnel lens that has been surface micromachined in polysilicon and then erected using hinge structures and locked in place using micromachined tabs, thus liberating the structure from the horizontal plane of the wafer [8.40, 42]. Various microactuators (e.g., comb drive, and vibromotors) have been used to move these structures out of the silicon plane and into position. Figure 8.36 shows an SEM photograph of a bar-code microscanner using a silicon optical microbench with 3-D surface-micromachined structures.

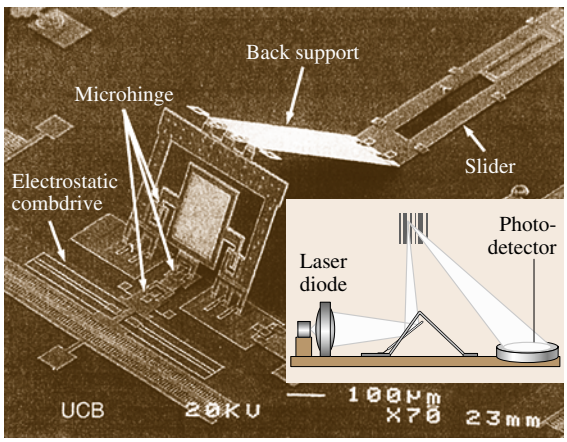

Fig. 8.36 Silicon pin-and-sample hinge scanner with 3-D surface-micromachined structures (after [8.40])

8.2.3 High-Aspect-Ratio Micromachining

The bulk and surface micromachining technologies presented in the previous sections fulfill the requirements of a large group of applications. Certain applications, however, require the fabrication of high-aspect-ratio structures that is not possible with the aforementioned technologies. In this section, we describe three technologies, LIGA, HEXSIL, and HARPSS, capable of producing structures with vertical dimensions much larger than their lateral dimensions by means of x-ray lithography (LIGA) and DRIE etching (HEXSIL and HARPSS).

LIGA

LIGA is a high-aspect-ratio micromachining process which relies on x-ray lithography and electroplating (in German: *Lithographie*, *Galvanoformung*, *Abformung*) [8.43, 44]. We already introduced the concept of the plating-through-mask technique in *Surface Micromachining* (Fig. 8.10). With standard UV photolithography and photoresists, the maximum thickness achievable is on the order of a few tens of microns and the resulting metal structures show tapered walls. LIGA is a technology based on the same plating-through-mask idea but can be used to fabricate metal structures of thickness ranging from a few microns to a few millimeters with almost vertical side-walls. This is achieved using x-ray lithography and special photoresists. Due to their short wavelength, x-rays are able to penetrate through a thick photoresist layer with no scattering and define features with lateral dimensions down to 0.2 µm (aspect ratio $> 100 : 1$).

The photoresists used in LIGA should comply with certain requirements, including sensitivity to x-rays, resistance to electroplating chemicals, and good adhesion to the substrate. Based on such requirements poly-(methyl methacrylate) (PMMA) is considered to be an optimal choice for the LIGA process. Application of the thick photoresist on top of the substrate can be performed by various techniques such as multiple spin-coating, precast PMMA sheets, and plasma polymerization coating. The mask structure and materials for x-ray lithography must also comply with certain requirements. The traditional masks based on glass plates with a patterned chrome thin layer are not suitable be-

Fig. 8.37 SEM of assembled LIGA-fabricated nickel structures (after [8.44])

cause x-rays are not absorbed by the chromium layer and the glass plate is not transparent enough. Instead, x-ray lithography uses a silicon nitride mask with gold as the absorber material (typically formed by electroplating gold to a thickness of 10–20 µm). The nitride membrane is supported by a silicon frame which can be fabricated using bulk micromachining techniques. Once the photoresist is exposed to the x-rays and developed, the process proceeds with electroplating of the desired metal. Ni is the most commonly used, although other metals and metallic compounds such us Cu, Au, NiFe, and NiW are also electroplated in LIGA processes. Good agitation of the plating solution is the key to obtaining a uniform and repeatable result during this step. A paddle plating cell, based on a windshield-wiper-like device moving only a millimeter away from the substrate surface, provides extremely reproducible agitation. Figure 8.37 shows an SEM of a LIGA microstructure fabricated with electroplating nickel.

Due to the high cost of the x-ray sources (synchrotron radiation), LIGA technology was initially intended for the fabrication of molds that could be used many times in hot-embossing or injection-molding processes. However, it has been also used in many applications to directly form high-aspect-ratio metal structures on top of a substrate. A cheaper alternative to the LIGA process (with somehow poorer qualities) called UV-LIGA or *poor man's LIGA* has been proposed [8.45, 46]. This process uses SU-8 negative photoresists (available for spin-coating at various thickness ranging from 1 to 500 µm) and standard contact lithography equipment. Using this technique, aspect ra-

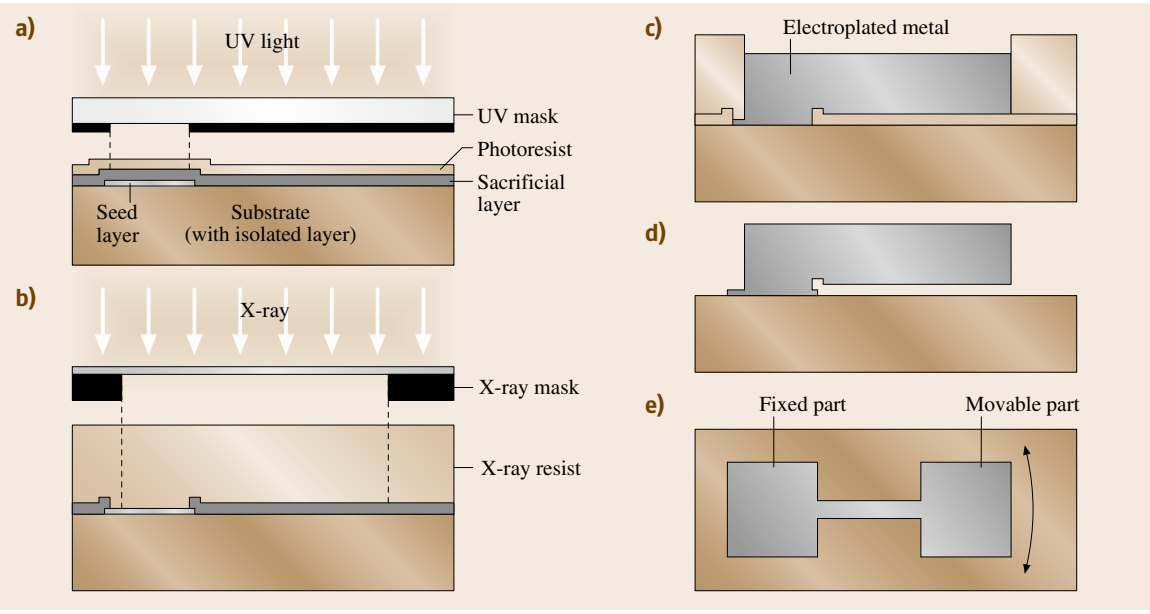

Fig. 8.38a–e Sacrificial LIGA process: **(a)** UV lithography for sacrificial layer patterning, **(b)** x-ray lithography, **(c)** electroplating, **(d)** structure releasing, and **(e)** top view of the movable structure

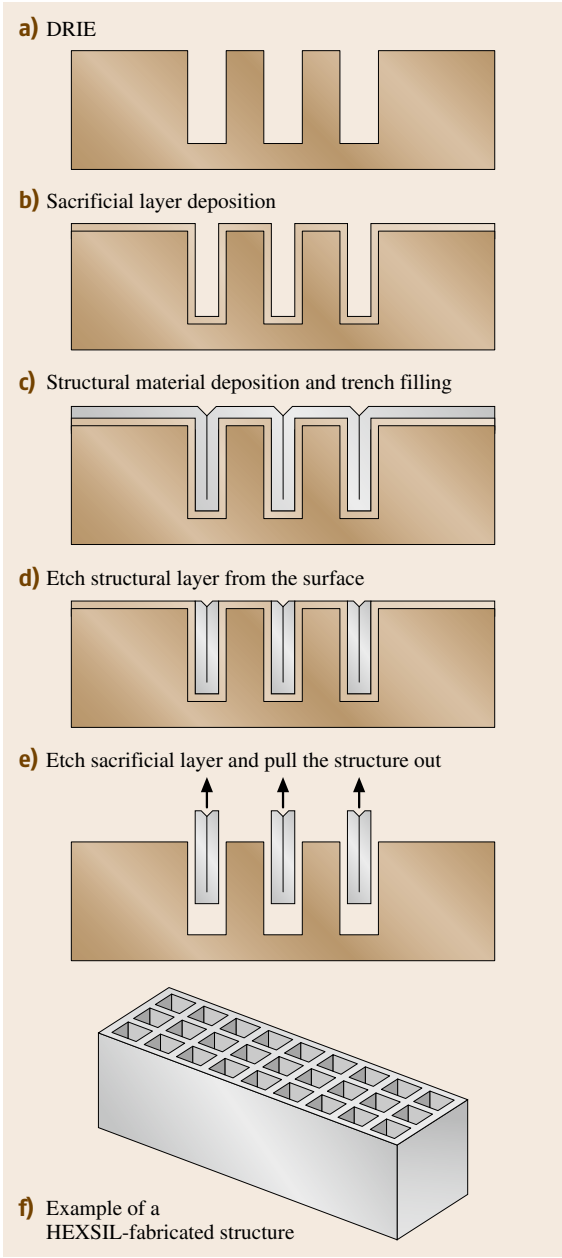

Fig. 8.39a–f HEXSIL process flow: (**a**) DRIE, (**b**) sacrificial layer deposition, (**c**) structural material deposition and trench filling, (**d**) etch structural layer from the surface, (**e**) etch sacrificial layer and pull the structure out, and (**f**) example of a HEXSIL-fabricated structure

tios larger than 20 : 1 have been demonstrated. A major problem of this alternative is the removal of the SU-8 photoresist after plating. Various methods, showing different degrees of success, have been proposed. These include: wet etching with special solvents, burning at high temperatures (600 °C), dry etching, use of a release layer, and high-pressure water-jet etching.

A variation of the basic LIGA process, shown in Fig. 8.38, permits the fabrication of electrically isolated movable structures, and thus opens more possibilities for sensor and actuator design using this technology [8.48]. This so-called sacrificial LIGA (SLIGA) starts with the patterning of the seed layer. Subsequently a sacrificial layer (e.g., titanium) is deposited and patterned. The process then proceeds as in standard LIGA until the last step, when the sacrificial layer is removed. The electroplated structures that overlap with the sacrificial layer are released in this step.

HEXSIL

The second method for fabricating high-aspect-ratio structures, which is based on a template replication technology, is hexagonal honeycomb polysilicon (HEXSIL) [8.49]. Figure 8.39 shows a simplified process flow. A high-aspect-ratio template is first formed in a silicon substrate using DRIE. Next, a sacrificial multilayer is deposited to allow the final release of the structures. The multilayer is composed of one or more PSG nonconformal layers to provide fast etch release ($\approx 20\,\mu m$/min in 49% HF) alternated with conformal layers of either oxide or nitride to provide enough thickness for proper release of the structures. The total thickness of the sacrificial layer has to be larger than the shrinkage or elongation of the structures caused by

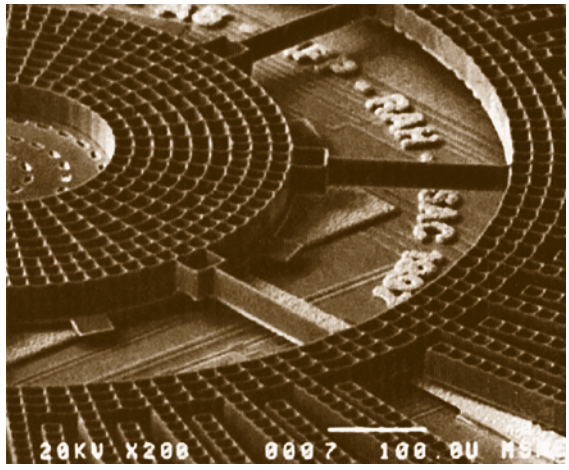

Fig. 8.40 SEM micrograph of an angular microactuator fabricated using the HEXSIL process (after [8.47])

the relaxation of the internal (compressive or tensile) stress during the release step. Otherwise the structures will clamp themselves to the walls of the template and their retrieval will not be possible. Any material that can be conformally deposited and yet not damaged during the HF release step is suitable for the structural layer. Structures made of polysilicon, nitride, and electroless nickel [8.50] have been reported. Nickel can only be deposited in combination with polysilicon since a conductive surface is needed for the deposition to occur. After deposition of structural materials a blanket etch (poly-Si or nitride) or a mechanical lapping (nickel) is performed to remove the excess materials from the surface. Finally, a 49% HF with surfactant is used to dissolve the sacrificial layers. The process can be repeated many times using the same template, thus considerably lowering fabrication costs. Figure 8.40 shows an SEM photograph of a microactuator fabricated using the HEXSIL process.

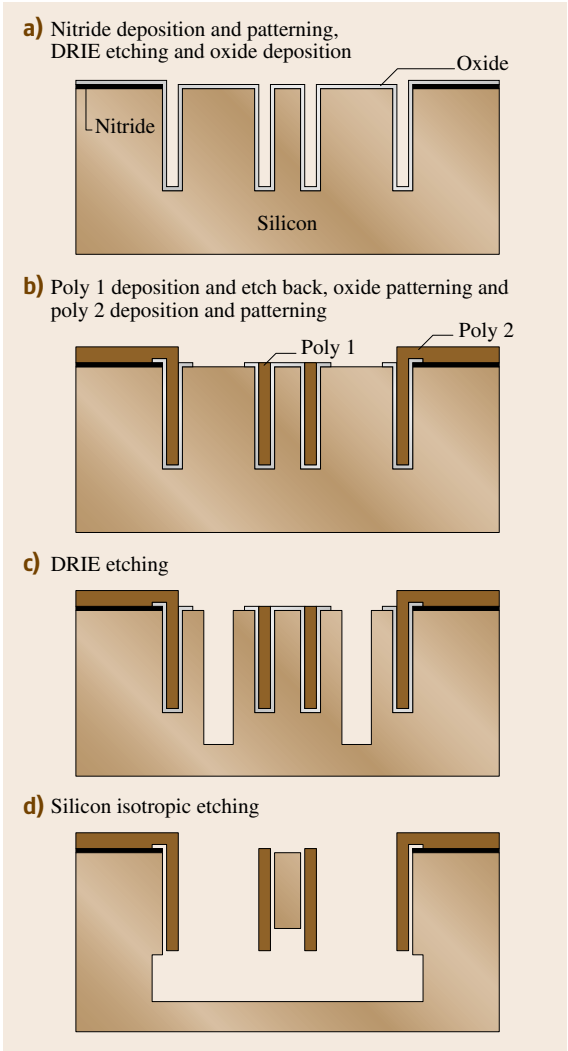

Fig. 8.41a–d HARPSS process flow: **(a)** nitride deposition and patterning, DRIE etching and oxide deposition, **(b)** poly 1 deposition and etch back, oxide patterning, and poly 2 deposition and patterning, **(c)** DRIE etching, and **(d)** silicon isotropic etching

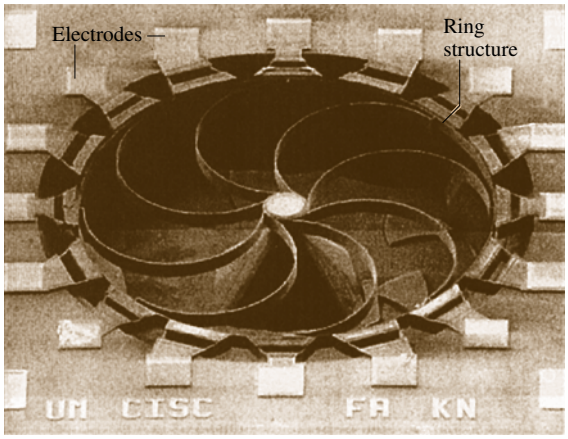

Fig. 8.42 SEM photograph of a microgyroscope fabricated using the HARPSS process (after [8.51])

HARPSS

The high-aspect-ratio combined poly- and single-crystal silicon (HARPSS) technology is another technique capable of producing high-aspect-ratio electrically isolated polycrystalline and single-crystal silicon microstructures with capacitive air gaps ranging from submicrometer to tens of micrometers [8.52]. The structures, tens to hundreds of micrometers thick, are defined by trenches etched with DRIE and filled with oxide and poly layers. The release of the microstructures is done at the end by means of a directional silicon etch followed by an isotropic etch. The small vertical gaps and thick structures possible with this technology find application in the fabrication of a variety of MEMS devices, particularly inertial sensors [8.53] and RF beam resonators [8.54]. Figure 8.41 shows the process flow in a cross section of a single-crystal silicon beam resonator. The HARPSS process starts with deposition and patterning of a silicon nitride layer that will be used to isolate the poly structure's connection pads from the substrate. High-aspect-ratio trenches ($\approx 5\,\mu m$ wide) are then etched into the substrate using a DRIE etch. Next,

a conformal oxide layer (LPCVD) is deposited. This layer has two functions, to:

1. Protect the structures during the dry etch release
2. Define the submicrometer gap between silicon and polysilicon structures

Following the oxide deposition, the trenches are completely filled with LPCVD polysilicon. The polysilicon is etched back and the underlying oxide is patterned to provide anchor points for the structures. A second layer of polysilicon is then deposited and patterned. Finally, the structures are released using a DRIE step followed by an isotropic silicon etch through a photoresist mask that exposes only the areas of silicon substrate surrounding the structures. It should be noted that single-crystal silicon structures are not protected at the bottom during the isotropic etch. This causes the single-crystal silicon structures to be etched vertically from the bottom, and thus be shorter than the polysilicon structures. Figure 8.42 shows an SEM photograph of a microgyroscope fabricated using the HARPSS process.

8.3 Nanofabrication Techniques

The microfabrication techniques discussed so far were mostly geared towards fabricating devices in the 1 mm to 1 μm dimensional range (submicrometer dimensions being possible in certain techniques such as HARPSS using a dielectric sacrificial layer). Recent years have witnessed a tremendous surge of interest in fabricating submicro- (1 μm–100 nm) and nanostructures (100–1 nm range) [8.55]. This interest arises from both practical and fundamental viewpoints. At the more scientific and fundamental level, nanostructures provide an interesting tool for studying the electrical, magnetic, optical, thermal, and mechanical properties of matter at the nanometer scale. These include important quantum-mechanical phenomena (e.g., conductance quantization, bandgap modification, coulomb blockade, etc.) arising from confinement of charged carriers in structures such as quantum wells, wires, and dots (Fig. 8.43). On the practical side, nanostructures can provide significant improvements in the performance of electronic/optical devices and sensors. In the device area investigators have been mostly interested in fabricating nm-sized transistors in anticipation of technical difficulties forecasted in extending Moore's law beyond 32 nm resolution. In addition, optical sources and detectors having nm-size dimensions exhibit improved characteristics not achievable in larger devices (e.g., lower threshold current, improved dynamic behavior, and improved emission line width in quantum dot lasers). These improvements create novel possibilities for next-generation computation and communication devices. In the sensors area, shrinking dimensions beyond conventional optical lithography can provide major improvements in sensitivity and selectivity.

One can broadly divide various nanofabrication techniques into top-down and bottom-up categories. The first approach starts with a bulk or thin-film material and removes selective regions to fabricate nanostructures (similar to micromachining techniques). The second method relies on molecular recognition and self-assembly to fabricate nanostructures out of smaller building blocks (molecules, colloids, and clusters). As can be anticipated, the top-down approach is an off-shoot of standard lithography and micromachining techniques. On the other hand, the bottom-up approach has a more chemical engineering and material science flavor and relies on fundamentally different principles. In this chapter, we will discuss several nanofabrication

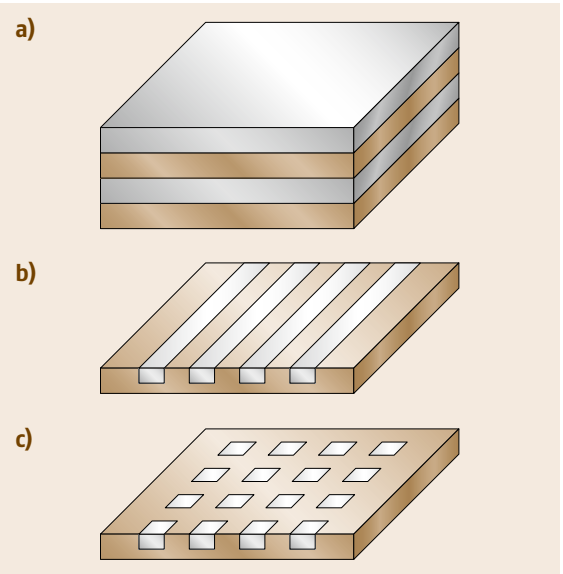

Fig. 8.43a–c Several important quantum confinement structures: **(a)** quantum well, **(b)** quantum wire, and **(c)** quantum dot

techniques that are not covered in other chapters of this Handbook. These include:

1. E-beam nanofabrication
2. Epitaxy and strain engineering
3. Scanning-probe techniques
4. Self-assembly and template manufacturing

8.3.1 E-Beam Nanofabrication

In previous sections, we discussed several important lithography techniques used commonly in MEMS and microfabrication. These included various forms of UV (regular, deep, and extreme) and x-ray lithography. However, due to the lack of resolution (in case of the UV) or difficultly in manufacturing mask and radiation sources (x-ray), these techniques are not suitable for nm-scale fabrication. E-beam lithography is an alternative and attractive technique for fabricating nanostructures [8.56]. It uses an electron beam to expose an electron-sensitive resist such as poly(methyl methacrylate) (PMMA) dissolved in trichlorobenzene (positive) or polychloromethylstyrene (negative) [8.57]. The e-beam gun is usually part of a scanning electron microscope (SEM), although transmission electron microscopes (TEM) can also be used. Although electron wavelengths of the order of 1 Å can be easily achieved, electron scattering in the resist limits the attainable resolutions to > 10 nm. Beam control and pattern generation is achieved through a computer interface. E-beam lithography is serial and hence has low throughput. Although this is not a major concern in fabricating devices used in studying fundamental microphysics, it severely limits large-scale nanofabrication. E-beam lithography in conjunction with processes such as lift-off, etching, and electrodeposition can be used to fabricate various nanostructures.

8.3.2 Epitaxy and Strain Engineering

Atomic-precision deposition techniques such as molecular-beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD) have proven to be effective tools in fabricating a variety of quantum confinement structures and devices (quantum well lasers, photodetector, resonant tunneling diodes, etc.) [8.58–60]. Although quantum wells and superlattices are the structures that lend themselves most easily to these techniques (Fig. 8.43a), quantum wires and dots have also been fabricated by adding subsequent steps such as etching and selective growth. Fabrication of quantum well and superlattice structures using epitaxial growth is a mature and well-developed field and therefore will not be discussed in this chapter. Instead, we will concentrate on quantum wire and dot nanostructure fabrication using basic epitaxial techniques [8.61, 62].

Quantum Structure Nanofabrication Using Epitaxy on Patterned Substrates

There have been several different approaches to the fabrication of quantum wires and dots using epitaxial layers. The most straightforward technique involves e-beam lithography and etching of an epitaxial grown layer (e.g., InGaAs on GaAs substrate) [8.63]. However, due to damage and/or contamination during lithography, this method is not very suitable for active device fabrication (e.g., quantum dot lasers). Several other methods involving regrowth of epitaxial layers over nonplanar surfaces such as step-edge, cleaved-edge, and patterned substrate have been used to fabricate quantum wires and dots without the need for lithography and etching of the quantum confinement structure [8.62, 64]. These nonplanar surface templates can be fabricated in a variety of ways such as etching through a mask or cleavage along crystallographic planes. Subsequent epitaxial growth on top of these structures results in a set of planes with different growth rates depending on the geometry or surface diffusion and adsorption effects. These effects can significantly enhance or limit the growth rate on certain planes, resulting in lateral patterning and confinement of deposited epitaxial layers and formation of quantum wires (in V-grooves) and dots

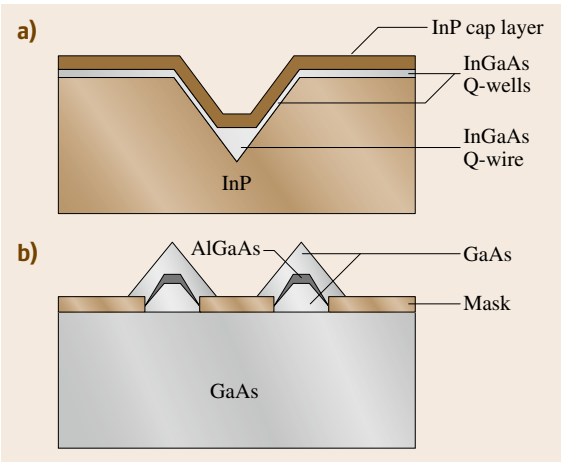

Fig. 8.44 **(a)** InGaAs quantum wire fabricated in V-groove InP, and **(b)** AlGaAs quantum wire fabricated by epitaxial growth on a masked GaAs substrate

(in inverted pyramids). Figure 8.44a shows a schematic cross section of an InGaAs quantum wire fabricated in a V-groove in InP. As can be seen the growth rate on the side-walls is lower than that of the top and bottom surfaces. Therefore the thicker InGaAs layer at the bottom of the V-groove forms a quantum wire confined from the sides by a thinner layer having a wider bandgap. Figure 8.44b shows a quantum wire formed using epitaxial growth over a dielectric patterned planar substrate. In both of these techniques it is relatively easy to create quantum wells; however, in order to create quantum wires and dots one still needs e-beam lithography to pattern the grooves and window templates.

Quantum Structure Nanofabrication Using Strain-Induced Self-Assembly

A more recent technique for fabricating quantum wires and dots involves strain-induced self-assembly [8.62, 65]. The term *self-assembly* represents a process where a strained two-dimensional (2-D) system reduces its energy by a transition into a 3-D morphology. The most commonly used material combination for this technique is the $In_xGa_{1-x}As/GaAs$ system, which offers a large lattice mismatch (7.2% between InAs and GaAs) [8.66, 67], although recently Ge dots on Si substrate have also attracted considerable attention [8.68]. This method relies on lattice mismatch between an epitaxially grown layer and its substrate to form an array of quantum dots or wires. Figure 8.45 shows a schematic of the strain-induced self-assembly process. When the lattice constant of the substrate and the epitaxial layer differ considerably, only the first few deposited monolayers crystallize, in the form of an epitaxial strained layer in which the lattice constants are equal. When a critical thickness is exceeded, a significant strain that occurs in the layer leads to the breakdown of this ordered structure and to the spontaneous formation of randomly distributed islets of regular shape and similar size (usually < 30 nm in diameter). This mode of growth is usually referred to as the Stranski–Krastanow mode. The quantum dot size, separation, and height depend on the deposition parameters (i. e., total deposited material, growth rate, and temperature) and material combinations. As can be seen, this is a very convenient method to grow perfect crystalline nanostructures over a large area without any lithography and etching. One major drawback of this technique is the randomness of the quantum dot distribution. It should be mentioned that this technique can also be used to fabricate quantum wires by strain relaxation bunching at step edges.

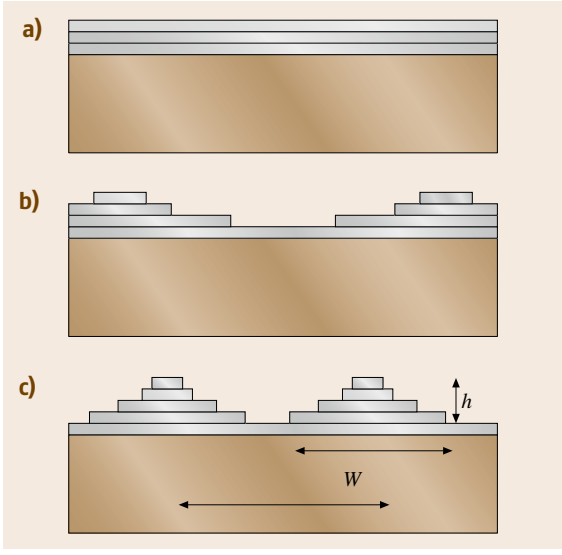

Fig. 8.45a–c Stranski–Krastanow growth mode, **(a)** 2-D wetting layer, **(b)** growth front roughening and breakup, and **(c)** coherent 3-D self-assembly

8.3.3 Scanning Probe Techniques

The invention of scanning probe microscopy in the 1980s revolutionized atomic-scale imaging and spectroscopy. In particular scanning tunneling and atomic force microscopes (STM and AFM) have found widespread applications in physics, chemistry, material science, and biology. The possibility of atomic-scale manipulation, lithography, and nanomachining using such probes was considered from the beginning and has matured considerably over the past decade. In this section after a brief introduction to scanning probe microscopes, we will discuss several important nanolithography and machining techniques which have been used to create nm-sized structures.

Scanning probe microscopy (SPM) systems are capable of controlling the movement of an atomically sharp tip in close proximity to or in contact with a surface with subnanometer accuracy. Piezoelectric positioners are typically used in order to achieve such accuracy. High-resolution images can be acquired by raster scanning the tips over a surface while simultaneously monitoring the interaction of the tip with the surface. In scanning tunneling microscope systems a bias voltage is applied to the sample and the tip is positioned close enough to the surface that a tunneling current develops through the gap (Fig. 8.46a). Because this current is extremely sensitive to the distance between the

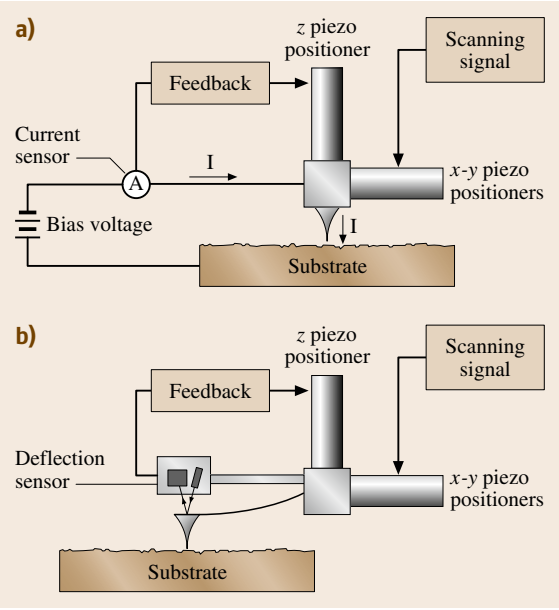

Fig. 8.46a,b Scanning probe systems: **(a)** STM and **(b)** AFM

tip and the surface, scanning the tip in the x–y-plane while recording the tunnel current permits the mapping of the surface topography with resolution on the atomic scale. In a more common mode of operation the amplified current signal is connected to the z-axis piezoelectric positioner through a feedback loop so that the current and therefore the distance are kept constant throughout the scanning. In this configuration the picture of the surface topography is obtained by recording the vertical position of the tip at each x–y-position.

The STM system only works for conductive surfaces because of the need to establish a tunneling current. The atomic force microscopy was developed as an alternative for imaging either conducting or nonconducting surfaces. In AFM the tip is attached to a flexible cantilever and is brought into contact with the surface (Fig. 8.46b). The force between the tip and the surface is detected by sensing the cantilever deflection. A topographic image of the surface is obtained by plotting the deflection as a function of the x–y-position. In a more common mode of operation a feedback loop is used to maintain a constant deflection while the topographic information is obtained from the cantilever vertical displacement. Some scanning probe systems use a combination of the AFM and the STM modes, i. e., the tip is mounted on a cantilever with electrical connection so that both the surface forces and tunneling currents can be controlled or monitored. STM systems can be operated in ultrahigh vacuum (UHV STM) or in air, whereas AFM systems are typically operated in air. When a scanning probe system is operated in air, water adsorbed onto the sample surface accumulates underneath the tip, forming a meniscus between the tip and the surface. This water meniscus plays an important role in some of the scanning probe techniques described below.

Scanning-Probe-Induced Oxidation

Nanometer-scale local oxidation of various materials can be achieved using scanning probes operating in air and biased at a sufficiently high voltage (Fig. 8.47). A tip bias of -2 to -10 V is normally used, with a writing speed of 0.1–100 µm/s in ambient humidity of 20–40%. It is believed that the water meniscus formed at the contact point serves as an electrolyte such that the biased tip anodically oxidizes a small region of the surface [8.70]. The most common application of this principle is the oxidation of hydrogen-passivated silicon. A dip in HF solution is typically used to passivate the silicon surfaces with hydrogen atoms. Patterns of oxide *written* on a silicon surface can be used as a mask for wet or dry etching. Patterns with 10 nm line width have been successfully transferred to a silicon substrate in this fashion [8.71]. Various metals have also been locally anodized using this approach, such us aluminum or titanium [8.72]. An interesting variation of this process is anodization of deposited amorphous silicon [8.73]. Amorphous silicon can be deposited at low

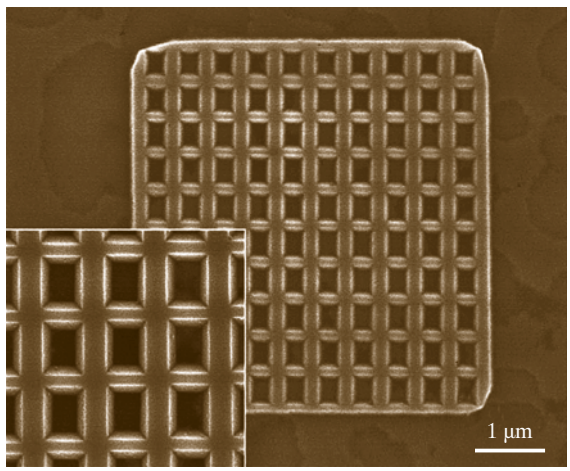

Fig. 8.47 SEM image of an inverted truncated pyramid array fabricated on a silicon SOI wafer by SPM oxidation and subsequent etch in TMAH (pitch is 500 nm) (after [8.69])

temperature on top of many materials. The deposited silicon layer can be patterned and used as, for example, the gate of a 0.1 μm CMOS transistor [8.74], or it can be used as a mask to pattern an underlying film. The major drawback of this technique is poor reproducibility due to tip wear during the anodization. However, using AFM in noncontact mode has proved to overcome this problem [8.70].

Probe Resist Exposure and Lithography

Electrons emitted from a biased SPM tip can be used to expose a resist in the same way e-beam lithography that does (Fig. 8.48) [8.74]. Various systems have been used for this lithographic technique; these include constant-current STM, noncontact AFM, and AFM with constant tip–resist force and constant current. The systems using AFM cantilevers have the advantage that they can perform imaging and alignment tasks without exposing the resist. Resists well characterized for e-beam lithography (e.g., PMMA or SAL601) have been used with scanning probe lithography to achieve reliable sub-100 nm lithography. The procedure for this process is as follows. The wafers are cleaned and the native oxide (in the case of silicon or poly) is removed with a HF dip. Subsequently 35–100 nm-thick resist is spin-coated on top of the surface. The exposure is done by moving the SPM tip over the surface while applying a bias voltage sufficiently high to produce emission of electrons from the tip (a few tens of volts). Development of the resist is performed in standard solutions following the exposure. Features below 50 nm in width have been achieved with this procedure.

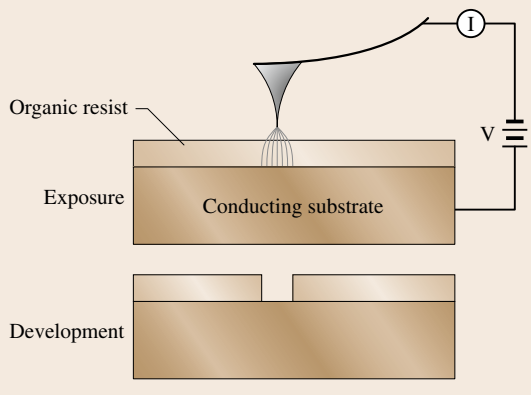

Fig. 8.48 Scanning probe lithography with organic resist

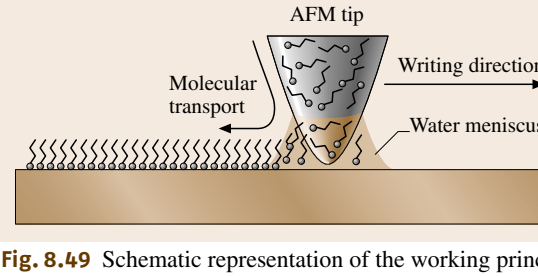

Fig. 8.49 Schematic representation of the working principle of dip-pen nanolithography

Dip-Pen Nanolithography

In dip-pen nanolithography (DPN) the tip of an AFM operated in air is *inked* with a chemical of interest and brought into contact with a surface. The ink molecules flow from the tip onto the surface as with a fountain pen. The water meniscus that naturally forms between the tip and the surface enables the diffusion and transport of the molecules, as shown in Fig. 8.49. Inking can be done by dipping the tip into a solution containing a low concentration of the molecules followed by a drying step (e.g., blow-drying with compressed difluoroethane). Line widths down to 12 nm with spatial resolution of 5 nm have been demonstrated with this technique [8.75]. Species patterned with DPN include conducting polymers, gold, dendrimers, DNA, organic dyes, antibodies, and alkanethiols. Alkanethiols have been also used as an organic monolayer mask to etch a gold layer and subsequently etch the exposed silicon substrate. One can also use a heated AFM cantilever to control the deposition of a solid organic ink. This technique was recently reported by *Sheehan* et al. in which 100 nm lines of octadecylphosphonic acid (melting point 100 °C) were written using a heated AFM probe [8.76].

Other Scanning Probe Nanofabrication Techniques

A great variety of nanofabrication techniques using scanning probe systems have been demonstrated. Some of these are proof-of-concept demonstrations and their utility as viable and repeatable fabrication processes has yet to be evaluated. For example, a substrate can be mechanically machined using a STM/AFM tip acting as a plow or engraving tool [8.77]. This can be used to create structures directly in the substrate, although it is more commonly used to pattern resist for a subsequently etch, lift-off or electrodeposition step. Mechanical nanomachining with SPM probes can be facilitated by heating the tip above the glass-transition temperature of a polymeric substrate material. This approach has been applied to SPM-based high-density data storage in polycarbonate substrates [8.78].

Electric fields strong enough to induce the emission of atoms from the tip can be easily generated by applying voltage pulses above 3 V. This phenomenon has been used to transfer material from the tip to the surface and vice versa. Mounds (10–20 nm) of metals such as Au, Ag, and Pt have been deposited or removed from a surface in this fashion [8.79]. The same approach has been used to extract single atoms from a semiconductor surface and redeposit them elsewhere [8.80]. Manipulation of nanoparticles, molecules, and single atoms on top of a surface has also been achieved by simply pushing or sliding them with the SPM tip [8.81]. Metals can also be locally deposited by the STM chemical vapor deposition technique [8.82]. In this technique a precursor organometallic gas is introduced into the STM chamber. A voltage pulse applied between the tip and the surface dissociates the precursor gas into a thin layer of metal. Local electrochemical etching [8.83] and electrodeposition [8.84] is also possible using SPM systems. A droplet of suitable solution is first placed on the substrate. Then the STM tip is immersed into the droplet and a voltage is applied. In order to reduce Faradaic currents the tip is coated with wax such that only the very end is exposed to the solution. Sub-100 nm feature size has been achieved using this technique.

Using a single tip to serially produce the desired modification in a surface leads to very slow fabrication processes that are impractical for mass production. Many of the scanning probe techniques developed so far, however, could also be performed by an array of tips, which would increase throughput and make them more competitive compared with other parallel nanofabrication processes. This approach has been demonstrated for imaging, lithography [8.85], and data storage [8.86] using both one- and two-dimensional arrays of scanning probes. With the development of larger arrays with advances in individual control of force, vertical position, and current, we might see these techniques being incorporated as standard fabrication processes in the industry.

8.3.4 Self-Assembly and Template Manufacturing

Self-assembly is a nanofabrication technique that involves aggregation of colloidal nanoparticles into the final desired structure [8.87]. This aggregation can be either spontaneous (entropic) and due to the thermodynamic minima (energy minimization) constraints or chemical and due to the complementary binding of organic molecules and supramolecules (molecular self-assembly) [8.88]. Molecular self-assembly is one of the most important techniques used in biology for the development of complex functional structures. Since these techniques require that the target structures be thermodynamically stable, it tends to produce structures that are relatively defect-free and self-healing. Self-assembly is by no means limited to molecules or the nanodomain and can be carried out on just about any scale, making it a powerful bottom-up assembly and manufacturing method (multiscale ordering). Another attractive feature of this technique relates to the possibility of combining self-assembly properties of organic molecules with the electronic, magnetic, and photonic properties of inorganic components. Template manufacturing is another bottom-up technique which utilizes material deposition (electroplating, CVD, etc.) into nanotemplates in order to fabricate nanostructures. Due to the simplicity and flexibility of electrochemistry for plating and surface finishing of a broad range of materials, its principle has recently been widely used for electrochemical fabrication of various metallic nanostructures based on various templates. For example, electrochemical deposition has been used to deposit large arrays of nanostructures in nanoporous templates, such as porous alumina. This template-based deposition typically provides metal nanowires as small as 25 nm in diameter and a few micrometers in length [8.89].

The nanotemplates used to fabricate nanostructures are usually prepared using self-assembly techniques. In the following sections, we will discuss various important self-assembly and template manufacturing techniques currently under heavy investigation.

Physical and Chemical Self-Assembly

The central theme behind the self-assembly process is spontaneous (physical) or chemical aggregation of colloidal nanoparticles [8.90]. Spontaneous self-assembly exploits the tendency of monodispersed nano or submicro colloidal spheres to organize into a face-centered cubic (fcc) lattice. The force driving this process is the desire of the system to achieve a thermodynamically stable state (minimum free energy). In addition to spontaneous thermal self-assembly, gravitational, convective, and electrohydrodynamic forces can also be used to induce aggregation into complex 3-D structures. Chemical self-assembly requires the attachment of a single-molecular organic layer (self-assembled monolayer or SAM) to the colloidal particles (organic or inorganic) and subsequent self-assembly of these components into a complex structures using molecular recognition and binding.

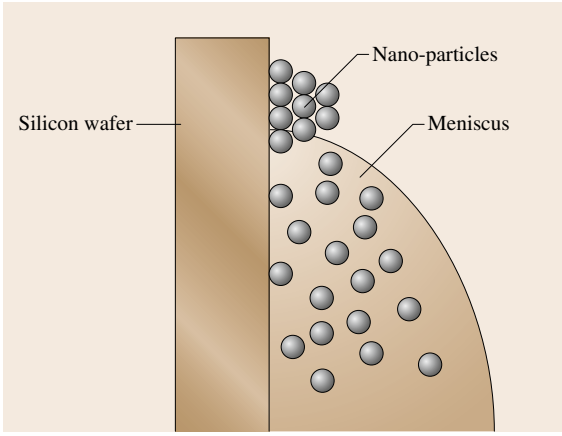

Fig. 8.50 Colloidal particle self-assembly onto solid substrates upon drying in vertical position

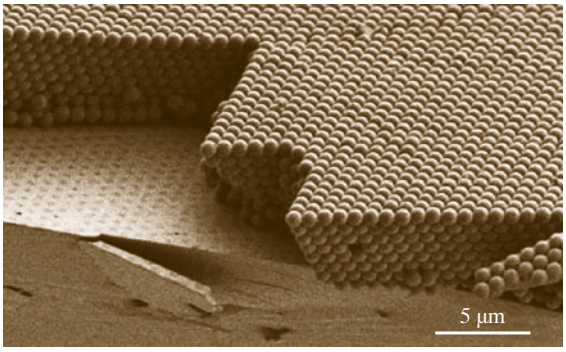

Fig. 8.51 Cross-sectional SEM image of a thin planar opal silica template (spheres 855 nm in diameter) assembled directly on a Si wafer (after [8.91])

Physical Self-Assembly

This is an entropy-driven method that relies on spontaneous organization of colloidal particles into a relatively stable structure through noncovalent interactions; for example, colloidal polystyrene spheres can be assembled into a 3-D structure on a substrate which is held vertically in the colloidal solution (Fig. 8.50) [8.91, 92]. Upon the evaporation of the solvent, the spheres aggregate into a hexagonal close-packed (hcp) structure. The interstitial pore size and density are determined by the polymer sphere size. The polymer spheres can be etched into smaller sizes after forming the hcp arrays, thereby altering the template pore separations [8.93]. This technique can fabricate large patterned areas in a quick, simple, and cost-effective way. A classic example is the natural assembly of on-chip silicon photonic-bandgap crystals [8.91] which are capable of reflecting the light arriving in any direction in a certain wavelength range [8.94]. In this method, a thin layer of silica colloidal spheres is assembled on a silicon substrate. This is achieved by placing a silicon wafer vertically in a vial containing an ethanolic suspension of silica spheres. A temperature gradient across the vial aids the flow of silica spheres. Figure 8.51 shows a cross-sectional SEM image of a thin planar opal template assembled directly on a Si wafer from 855 nm spheres. Once such a template is prepared, LPCVD can be used to fill the interstitial spaces with Si, so that the high refractive index of silicon provides the necessary bandgap.

One can also deposit colloidal particles onto a patterned substrate (template-assisted self-assembly, TASA) [8.95, 96]. This method is based on the principle that, when an aqueous dispersion of colloidal particles is allowed to dewet from a solid surface which is already patterned, the colloidal particles are trapped by the recessed regions and assemble into aggregates with shapes and sizes determined by the geometric confinement provided by the template. The patterned arrays of templates can be fabricated using conventional contact-mode photolithography which gives control over the shape and dimensions of the templates, thereby allowing the assembly of complex structures from colloidal particles. The cross-sectional view of a fluidic cell used in TASA is shown in Fig. 8.52. The fluidic cell has two parallel glass substrates to confine the aqueous dispersion of the colloidal particles. The surface of the bottom substrate is patterned with a 2-D array of templates. When the aqueous dispersion is allowed to dewet slowly across the cell, the capillary force exerted on the liquid pushes the colloidal spheres across the surface of the bottom substrate until they are physically trapped by the templates. If the concentration of the colloidal dispersion is high enough, the template will be filled by

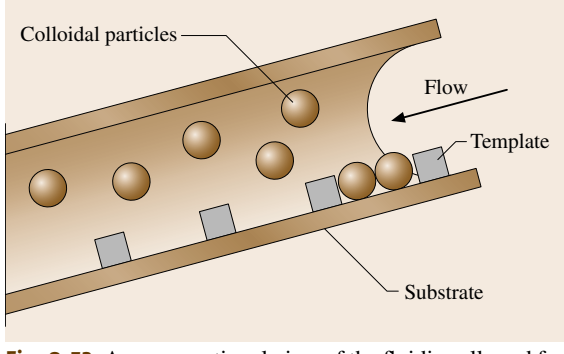

Fig. 8.52 A cross-sectional view of the fluidic cell used for template-assisted self-assembly

the maximum number of colloidal particles determined by the geometrical confinement. This method can be used to fabricate a variety of polygonal and polyhedral aggregates which are difficult to generate [8.97].

Chemical Self-Assembly

Organic and supramolecular SAMs play a critical role in colloidal particle self-assembly. SAMs are robust organic molecules which are chemically adsorbed onto solid substrates [8.98]. Most often they have a hydrophilic (polar) head which can be bonded to various solid surfaces and a long hydrophobic (nonpolar) tail which extends outward. SAMs are formed by the immersion of a substrate in a dilute solution of the molecule in an organic solvent or water (liquid phase) or by exposure to an atmosphere containing such a molecule (gas phase). The resulting film is a dense organization of molecules arranged to expose the end group. The durability of the SAM is highly dependent on the effectiveness of the anchoring to the surface of the substrate. SAMs have been widely studied because the end group can be functionalized to form precisely arranged molecular arrays for various applications ranging from simple, ultrathin insulators and lubricants to complex biological sensors. Chemical self-assembly uses organic or supramolecular SAMs as the binding and recognition sites for fabricating complex 3-D structures from colloidal nanoparticles. The most commonly used organic monolayers include:

1. Organosilicon compounds on glass and oxidized silicon
2. Alkanethiols, dialkyl disulfides, and dialkyl sulfides on gold
3. Fatty acids on alumina and other metal oxides
4. DNA

Octadecyltrichlorosilane (OTS) is the most common organosilane used in the formation of SAMs, mainly because of the fact that it is simple, readily available, and forms good, dense layers [8.99, 100]. Alkyltrichlorosilane monolayers can be prepared on clean silicon wafers whose surface is SiO_2 (with almost 5×10^{14} SiOH groups/cm^2). Figure 8.53 shows a schematic representation of the formation of alkylsiloxane monolayers by adsorption of alkyltrichlorosilane from solution onto Si/SiO_2 substrates. Since the silicon–chloride bond is susceptible to hydrolysis, a limited amount of water has to be present in the system in order to obtain good-quality monolayers. Monolayers made of methyl- and vinyl-terminated alkylsilanes are autophobic to the hydrocarbon solution and hence emerge uniformly dry from the solution, whereas monolayers made of ester-terminated alkylsilanes emerge wet from the solution used in their formation. The disadvantage of this method is that, if the alkyltrichlorosilane in the solvent adhering to the substrate is exposed to water, a cloudy film is deposited on the surface due to the formation of a gel of polymeric siloxane. One solution to this problem is the use of alkyldimethylchlorosilanes, which have a single anchoring point, and thus cannot form polymers. Chlorosilanes are sometimes preferred over alkoxysilanes because of their higher reactivity. However, the reactivity of chlorosilanes severely limits the range of functional groups that can be introduced at the end of the hydrocarbon tail. On the contrary, methoxysilanes and ethoxysilanes are commonly available with many functional groups including amino, mercapto, epoxy, and thiocyanate groups, which are often necessary for subsequent binding of colloidal particles and biomolecules. Gas-phase deposition of these molecules yields more uniform layers compared with liquid-phase procedures [8.101]. Soft-lithography-like molds have been used to obtain reactive silane patterns from the gas phase by taking advantage of the characteristic permeability of PDMS to volatile molecules [8.102].

Another important organic SAM system is the alkanethiols ($X(CH_2)_nSH$, where X is the end group) on gold [8.98, 103–105]. A major advantage of using gold as the substrate material is that it does not have a stable oxide and thus can be handled in ambient conditions. When a fresh, clean, hydrophilic gold substrate is im-

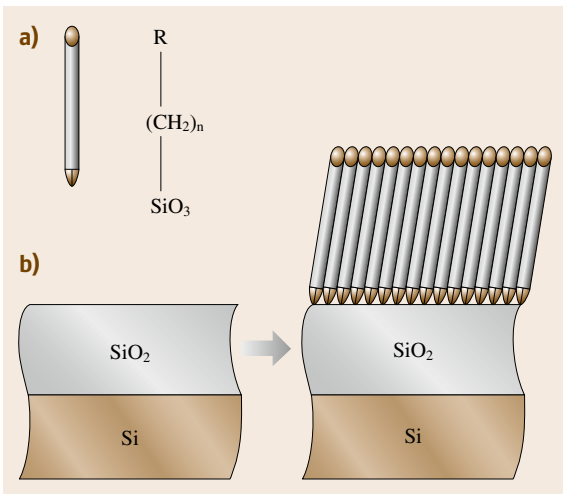

Fig. 8.53 **(a)** Alkylsiloxane formed from the adsorption of alkyltrichlorosilane on Si/SiO_2 substrates. **(b)** Schematic representation of the process

mersed (several min to several h) into a dilute solution (10^{-3} M) of the organic sulfur compound (alkanethiols) in an inorganic solvent a close-packed, oriented monolayers can be obtained. Sulfur is used as the head group because of its strong interaction with the gold substrate (44 kcal/mol), resulting in the formation of a close-packed, ordered monolayer. The end group of alkanethiol can be modified to render the adsorbed layer hydrophobic or hydrophilic. Another method for depositing alkanethiol SAM is soft lithography. This technique is based on inking a PDMS stamp with alkanethiol and its subsequent transfer to planar or nonplanar substrates. Alkanethiol-functionalized surfaces (planar, nonplanar, spherical) can also be used to self-assemble a variety of intricate 3-D structures [8.106].

Carboxylic acid derivatives self-assemble on surfaces (e.g., glass, Al_2O_3, and Ag_2O) through an acid–base reaction, giving rise to monolayers of fatty acids [8.107]. The time required for the formation of a complete monolayer increases with decreasing concentration. Higher concentration of the carboxylic acid is required to form a monolayer on gold as compared with on Al_2O_3. This is due to differences in the affinity of the COOH groups (more affinity to Al_2O_3 and glass than gold) and also the surface concentration of the salt-forming oxides of the two substrates. In the case of amorphous metal oxide surfaces, the chemisorption of alkanoic acids is not unique. For example, on Ag_2O, the two oxygen atoms of the carboxylate bind to the substrate in a nearly symmetrical manner, thus resulting in ordered monolayers with a chain tilt angle of 15−25° from the surface normal. However, on CuO and Al_2O_3, the oxygen atoms bind themselves symmetrically and the chain tilt angle is close to 0°. The structure of the monolayers is thus a balance of the various interactions taking place in the polymer chains.

Deoxyribonucleic acid (DNA), the framework on which all life is built, can be used to self-assemble nanomaterials into useful macroscopic aggregates that display a number of desirable physical properties [8.108]. DNA consists of two strands, which are coiled around each other to form a double helix. When the two strands are uncoiled singular strands of nucleotides are left. These nucleotides consist of a sugar (pentose ring) a phosphate (PO_4), and a nitrogenous base. The order and architecture of these components is essential for the proper structure of a nucleotide. There are typically four nucleotides found in DNA: adenine (A), guanine (G), cytosine (C), and thymine (T). A key property of the DNA structure is that the nucleotides described bind specifically to another nucleotide when arranged in the two-strand double helix (A to T, and C to G). This specific bonding capability can be used to assemble nanophase material and nanostructures [8.109]. For example, nucleotide-functionalized nanogold particles have been assembled into complex 3-D structures by attaching DNA strands to the gold via an enabler or linker [8.110]. In a separate work DNA was used to assemble nanoparticles into macroscopic materials. This method uses alkane dithiol as the linker molecule to connect the DNA template to the nanoparticle. The thiol groups at each end of the linker molecule covalently attach themselves to the colloidal particles to form aggregate structures [8.111].

Template Manufacturing

Template manufacturing refers to a set of techniques that can be used to fabricate 3-D organic or inorganic structures from a nanotemplate. These templates differ in material, pattern, feature size, overall template size, and periodicity. Although nanotemplates can be fabricated using e-beam lithography, the serial nature of this technique prohibits its widespread application. Self-assembly is the preferred technique to produce large-area nanotemplates in a massively parallel fashion. Several nanotemplates have been investigated for use in template manufacturing. These include polymer colloidal spheres, alumina membranes, and nuclear-track etched membranes. Colloidal spheres can be deposited in a regular 3-D array using the techniques described in the previous section (Figs. 8.50–8.52). Porous aluminum oxide membranes can be fabricated by the anodic oxidation of aluminum [8.112]. The oxidized film consists of columnar arrays of hexagonal close-packed pores with separation comparable to the pore size. By controlling the electrolyte species, temperature, anodizing voltage, and time, different pore sizes, densities, and heights can be obtained. The pore size and depth can further be adjusted by etching the oxide in an appropriate acid. Templates of porous polycarbonate or mica membranes can be fabricated by nuclear-track etched membranes [8.113]. This technique is based on the passage of high-energy decay fragments from a radioactive source through a dielectric material. The particles leave behind chemically active damaged tracks which can subsequently be etched to create pores through the thickness of the membrane [8.114, 115]. Unlike other methods, the pore separation and hence the pore density is independent of the pore size. The pore density is only determined by the irradiation process. More recently, electrochem-

ical deposition of metallic nanowires on the step edges of highly oriented pyrolytic graphite (HOPG) templates have also been demonstrated, which produces metallic nanowires with diameters as small as 15 nm. This method has been successfully used for metals such as Cu, Ni, Au, and Pd [8.116, 117].

Subsequent to template fabrication, the interstitial spaces (in the case of colloidal spheres) or pores (in the case of alumina and polycarbonate membranes) in the template are filled with the desired material [8.93, 118]. This can be done by using a variety of deposition techniques such as electroplating and CVD. The final structure can be a composite of nanotemplate and deposited material or the template can be selectively etched, resulting in an air-filled 3-D complex structure. For example, nickel [8.119], iron [8.120], and cobalt [8.121] nanowires have been electrochemically grown into porous template matrices. Three-dimensional photonic crystals have been fabricated by electrochemical deposition of CdSe and silicon into polystyrene and silica colloidal assembly templates [8.91, 122]. An interesting example of template-assisted manufacturing is the synthesis of nanometer metallic barcodes [8.123]. These nanobarcodes are prepared by electrochemical reduction of metallic ions into the pores of an aluminum oxide membrane, followed by their release through etching of the template [8.93].

8.4 Summary and Conclusions

In this chapter, we have discussed various micro/nanofabrication techniques used to manufacture structures of a wide range of dimensions (mm–nm). Starting with some of the most common microfabrication techniques (lithography, deposition, and etching), we have presented an array of micromachining and MEMS technologies which can be used to fabricate microstructures down to $\approx 1\,\mu m$. These techniques have attained an adequate level of maturity to enable a variety of MEMS-based commercial products (pressure sensors, accelerometers, gyroscopes, etc.). More recently, nm-size structures have attracted an enormous amount of interest. This is mainly due to their unique electrical, magnetic, optical, thermal, and mechanical properties. These could lead to a variety of electronic, photonic, and sensing devices with a superior performance compared with their macro counterparts. Subsequent to our discussion on MEMS and micromachining, we presented several important nanofabrication techniques currently under intense investigation. Although e-beam and other high-resolution lithography techniques can be used to fabricate nm-size structures, their serial nature and/or cost preclude their widespread application. This has forced investigators to explore alternative and potentially superior techniques such as strain engineering, self-assembly, and nanoimprint lithography. Among these self-assembly is the most promising method due to its low cost and the ability to produce nanostructures at different length scales.

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