Sunanda Babu

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SUMMARY: Seeking a satisfying and enriching role in your esteemed organisation

EDUCATION:

- 1993-1995 M.Tech Solid State Technology, IIT Chennai, India
- 1988-1993 M.Sc Chemistry(5 year Integrated) , IIT Kharagpur, India

WORK EXPERIENCE:

Apr 2015- Apr 2017 CeNSE, IISc Bangalore ***www.cense.iisc.ac.in***

Technology Manager, Thin Films, Dry Etch, Process Integration

- Lead the team to maintain the functionality of the process bays
- Motivate / Lead /Facilitate the team to resolve equipment and process issues
- Streamline existing processes/implement new systems and procedures for efficient and transparent execution of processes.
- Interact with external NNfC users and ensure quality and timely completion of their projects by facilitating with process integration team.
- Enhanced the coordination level between the various modules in NNfC on a team basis.

Jan2014- Mar 2015 SSMC, Singapore ***www.ssmc.com.sg***

Principal Engineer, Technology Development

- Project leader for 0.25um QUBIC4 +TF process transfer from ICN8 (NXP semiconductors) to SSMC, involves interaction and coordination with internal and external customers.
- Facilitated regular technical meetings with mother fab (ICN8).
- Ensured the timely achievement of project milestones.
- Problem solving and process optimisation (Temperature coefficient of resistance of SiCr resistor, VIA resistance improvement)

July 2012 – Dec 2013 NXP Semiconductors, Nijmegen ***www.nxp.com***

Process Integration Engineer

- Line sustaining and Process improvement activities to increase yield and reduce cycle time.
- Coordination and Interaction with all modules to drive improvement activities.

April 2010 – Aug 2010 GlobalFoundries, Singapore ***www.globalfoundries.com***

Customer Engineering Section Manager

- Responsible to manage the customer product life cycle.
- Facilitated regular teleconferences between customer and foundry teams to update / discuss product yields and low yield issues.

- Coordinated the turn-key related services with internal and external turnkey houses for customers.
- Coordinated timely preparation of SMP(supplier managemement program) booklet for distribution to all participants.

May 2008 - March 2010 SpectraLinear, India(now SiLabs) ***www.spectralinear.com***

Senior Engineer, Quality and Reliability Assurance

- Coordinated with Design, Test Engineering, Product Engineering, Planning, Sales and Suppliers on Failure analysis process for Customer rejects, prepared FA acknowledgement letters to send to customers on initial feedback of FA within 24 hours, prepared the FA report based on 8D for the customer within 2 weeks of receipt of failure parts.
- Administered RMA (return material authorization) for the failure parts, along with Planning and Finance teams.
- Managed the CAR process with internal and external suppliers (test houses, assembly houses, distributors). It included the investigation of potential causes of non-conforming product, disposition of non-conforming material and development of preventive and corrective actions to prevent similar non-conformances.
- Successfully completed the ISO9000:2000 series Auditor/ Lead Auditor Training course conducted by Moody International.(IRCA, UK certification).
- Worked with Suppliers (foundry, assembly houses and test houses) and generated the Monthly Supplier Quality Report for Management. Cpk for critical eTest and inline process parameters, process reliability performance, defect ppm levels, CAR incidences, RMA $ impact and on-time delivery were indices used to monitor the suppliers.

May 2000 - June 2007 SSMC, Singapore ***http://www.ssmc.com.sg/***

Senior Engineer II and I, Process Integration (Jun 2004 – June2007)

0.14,0.15,0.18,0.25um Logic CMOS processes

- Identified opportunities for Fab cycle time improvement and qualified them, for all technologies (removal of various redundant wet clean steps, removal of anneal steps, evaluating shorter process recipes for deposition , etch or diffusion)
- Performed experiments to improve the gate oxide integrity for the 0.25um PMU process.
- Monitored inline Key process parameters and alerted modules of drift, worked with modules to understand root cause and ensured that corrective and preventive actions are in place (inline CD for active, Poly , LIL , contact and metal , STI step height and trench depth, pre and post STI CMP thickness, ILD and IMD thickness)
- Monitored Electrical parameters (WAT) by SPC (Cp, CpK, OOC and OOS). Performed troubleshooting of OOS / OOC / CpK degradation with root cause understanding and established corrective and preventive actions for product portfolio, belonging to various technologies (parameters include NMOS and PMOS Isat, Vt and leakages, silicided and unsilicided active and poly resistances, LIL, via and contact resistances, metal sheet resistances, electrical CD, gate oxide thickness and inter level dielectric capacitances and thickness.).
- Worked on Yield improvement / yield excursion issues.(STI trench depth optimization to improve the product Vddmin performance thus improving yield, transistor performance

improvement to gain margin from yield roll-off areas, yield excursion issues involved identifying culprit tool, or chamber or process margin, line-stop and speedy implementation of containment / corrective actions to prevent recurrences)

- Performed new product optimization (matrix lot analysis) in terms of transistor performance. (Run engineering lot and identify the performance of the various transistors (NMOS and PMOS high performance, low leakage and thick gate transistor). Tuning of transistors was done, in order to move away from yield roll-off areas.)
- Ensured prototype success (KPI was on- time delivery with no WAT OOS)
- RDL (Re-distribution Layer) process option qualification for CMOS18 / CMOS18S Logic processes (this option is used in Flip Chip)
- LIL / Contact Module optimization for CMOS14, CMOS18/CMOS18S technologies. Used DOE, 8D and other 6 sigma tools. (this was a yield improvement project, in terms of defect control , and better etch selectivity and better material)
- 0.25um Silicide module optimisation
- Optimisation of the RPO module for sensitive products(in terms of silicided and unsilicided poly and active resistances, which in turn affect the analog product performance)
- Improving robustness of the LIL / Contact Module for SP18S and SP14 Logic processes
- Involved in Yield improvement for 0.25um PMU (power management unit) process.

Senior Engineer and Engineer, CVD (May 2000 – May 2004)

0.14, 0.15, 0.18, 0.25um Logic CMOS processes

- Line maintenance, which involved speedy and correct disposition of wafers, affected by either CVD or PVD equipment alarms.
- Troubleshoot OOC/ OOS and Defect Notices with minimal impact to tool uptime and process quality and prevent recurrences.
- Ran shift duty to support production.
- Improved line monitoring / detection effectiveness, using SPC (OOS, OOS, Cp and CpK).
- Formulated process troubleshooting guides.
- Started up, optimized and qualified IMD and inorganic BARC recipes for 0.18 and 0.22um processes on Applied Materials Centura Platform
- Worked on various activities like CVD CAPEX (Capability Extension project) Particle, film uniformity, tool uptime improvement activities using 6 sigma tools like 8D and FMEA, Cost reduction and WPH improvement.
- Trainer for CVD process and equipment new hires.
- Hands-on experience with AMAT Deposition tools (PECVD, HDP-CVD, PVD), Novellus oxide and W deposition, thickness measurement tools (KLA-Tencor), SP1 (particle monitoring) and Film Stress monitoring.

April 1995-April 2000 VLSI, ITI Bangalore, India

Executive Engineer (1995 –2000)

- Started-up and Qualified of IMD and Passivation processes for the 1 um CMOS technology, on Novellus Concept- One and relevant metrology tools.

TRAINING/WORKSHOPS

- Underwent training in Technical Writing and Technical Problem Solving, conducted by SIM and British Council, Singapore (2005) respectively.
- Attended a course in Project Management Methodologies, Tools and Techniques, conducted by IT Knowledge, Siemens Associated Training Centre, Singapore (2005).
- Attended in-house training for 8D Methodologies and SPC (2003).
- Training course for various AMAT Centura and Endura tools and AMAT Training Centre,Singapore(2001)
- Underwent three months training at ICN8 (formerly MOS34), Nijmegen, Holland, to assist in the start up of the first Philips Semiconductor Fabrication facility (2000).
- Underwent one month training at Novellus training facility in San Jose, California (1998).

AWARDS/PRIZES

- Outstanding Performer award, Process Integration, May 2005, SSMC for outstanding contribution to RDL.
- Institute Silver medal and General Proficiency Prize, 1993, IIT Kharagpur, India.
- KL Chopra award for best M.Sc project, 1993, IIT Kharagpur, India.

SKILLS:

- Good problem solving skills.
- Good communcation skills with colleagues and superiors.
- Microsoft Word, Excel, PowerPoint and Internet Explorer.
- Dependable, adaptable, dedicated, hardworking, team player, fast learner.